White Paper

Using Altera's 1.00-mm FineLine BGA Packages

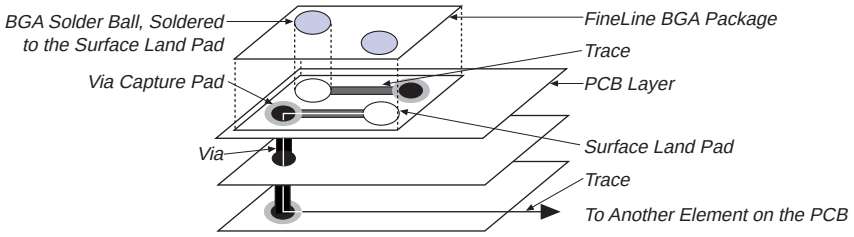
Altera has taken a leadership position in programmable logic device (PLD) packaging with the recent introduction of 1.00-mm FineLine BGA™ packages. These packages optimize the area on a printed circuit board (PCB) while maintaining a very high pin count. This white paper provides an overview of the PCB layout requirements to help you determine whether you can use FineLine BGA packages on your PCB.

Overview

When using ball-grid array (BGA) packages, there are several ways to route all signals to the system board without increasing PCB complexity and cost. With the increase in I/O counts, multi-layer PCBs have become an industry standard. BGA packages, with their matrix of solder balls across the bottom of the package, can use multi-layer PCB technology for escape routing—the method used to route each signal from a package to another element on the PCB. In multi-layered PCBs, signals are routed from the inner balls of the BGA package to various elements on the PCB through vias (or plated through-holes), which provide electrical connections between various PCB layers. To use 1.00-mm FineLine BGA packages, your PCB must have enough room for vias and escape routing. Figure 1 shows a sample signal traversing from a FineLine BGA solder ball to another element on the PCB.

Figure 1. Routing

A signal travels from a BGA solder ball to the surface land pad, to the trace, to the via capture pad, through the via, to the trace, and out to another element on the PCB.

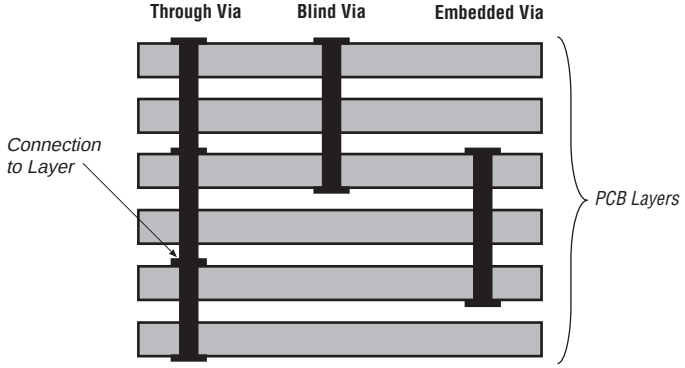


Vias

Multi-layered PCBs can contain three types of vias, as described below (see Figure 2).

- *Blind Via*—An interconnection between the top layer and an inner PCB layer.
- *Embedded Via*—An interconnection between any number of inner PCB layers.
- *Through Via*—An interconnection between the top and bottom layers of a PCB. The via may also include an interconnection between any number of inner PCB layers.

Figure 2. Types of Vias



Blind vias and through vias are more frequently used with 1.00-mm FineLine BGA packages than embedded vias. Blind vias can be more expensive than through vias, but overall costs can be reduced because signal traces can be routed under a blind via, requiring fewer PCB layers. Through vias, on the other hand, do not permit signals to be routed underneath layers, which can increase the required number of PCB layers and overall costs.

To see if enough space is available on your PCB for vias, you must determine:

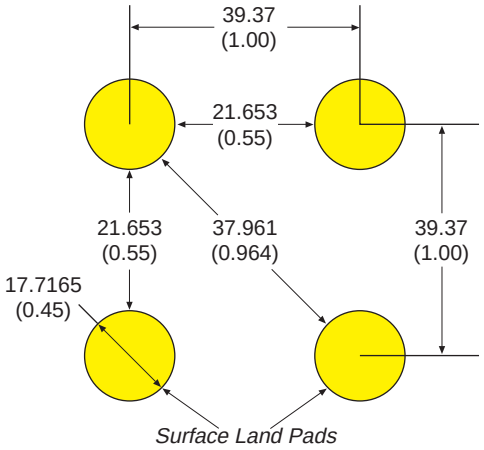
- The size of surface land pads
- The size and layout of via capture pads

Size of Surface Land Pads

The surface land pads are the areas on the PCB to which the BGA solder balls adhere. The size of these pads affects the space available for vias and escape routing. Altera recommends using a 17.7165-mil surface land pad, which is the same size as the BGA solder ball. Using a similarly sized pad balances the stress on the solder joint. Figure 3 shows how much space is available for vias and escape routing when you use 17.7165-mil surface land pads.

Figure 3. PCB Pad Layout

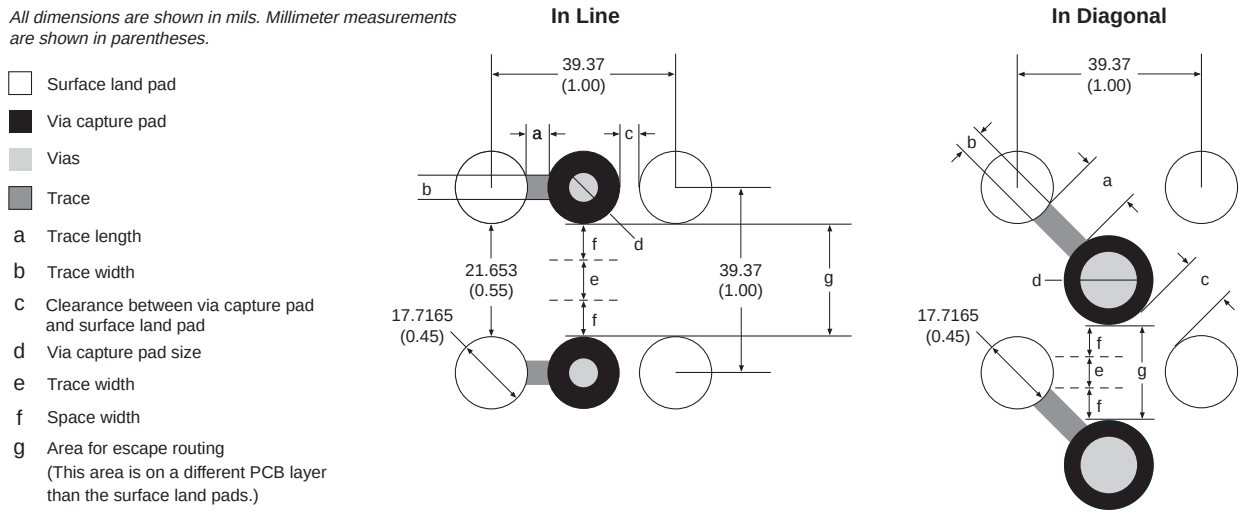
All dimensions are shown in mils. Millimeter measurements are shown in parentheses.



Size & Layout of Via Capture Pads

Vias are electrically connected to PCB layers through via capture pads, which also affect the amount of space available for vias and escape routing. Via capture pads can be laid out either in-line with the surface land pads or in the diagonal (see Figure 4).

Figure 4. Placement of Via Capture Pad



The decision to place a via capture pad in the diagonal or in-line with the surface land pads is based on the following criteria:

- Diameter of the via capture pad.
- Trace width and length.
- Clearance between the via capture pad and the surface land pad.

To determine if enough room is available to place via capture pads *in-line* with the surface land pads, use the following equation:

$a + c + d \leq 21.653$ mils

To determine if enough room is available to place via capture pads *in the diagonal* of the surface land pads, use the following equation:

$a + c + d \leq 37.961$ mils

If your PCB guidelines do not conform to either equation, contact Altera Applications at (800) 800-EPLD for further assistance.

Escape Routing

To perform escape routing, you must determine the width of the trace and the minimum space required between traces. The minimum space required for signal routing is the smallest space the signal must be routed through (i.e., the distance between two vias, or *g* in Figure 4). This dimension is calculated with the following formula:

$g = 39.37$ mils $- d$

The number of traces that can be routed through this space is based on the permitted line trace and space widths. For example, if the permitted line trace width is 4 mils and the space width is also 4 mils, the total space required is 12 mils (i.e., space width + trace width + space width). If *g* is 12 mils or greater, it is possible to route one trace. If *g* is less than 12 mils, you may not be able to use the 1.00-mm FineLine BGA package. Each PCB vendor has its own specification for via sizes, trace widths, and space widths. Depending on the specification, your escape routing can incorporate various numbers of traces between pads. Consult your PCB vendor for that company's specifications.

Table 1 shows how to determine the total number of traces that can be routed through *g*. In general, the number of traces is inversely proportional to the number of PCB layers required to route the package.

Table 1. Number of Trace Routed through g

Number of Traces	Formula
1	$g \geq [2 \times (\text{space width})] + \text{trace width}$
2	$g \geq [3 \times (\text{space width})] + [2 \times (\text{trace width})]$
3	$g \geq [5 \times (\text{space width})] + [3 \times (\text{trace width})]$

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