ALTERA®

Megafunctions Selector Guide

February 1998

Megafunctions Provide Total Solutions

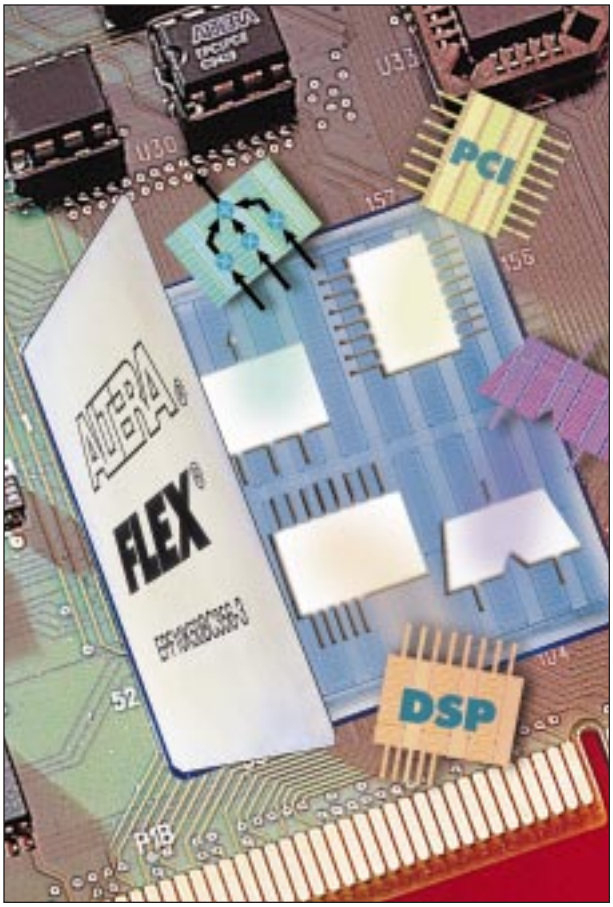
With programmable logic device (PLD) densities reaching 250,000 gates, it is now possible to implement entire digital subsystems within a single PLD. This new level in density creates greater opportunities for designers who are required to develop systems with higher integration, complexity, and functionality. Altera meets these opportunities directly by combining megafunctions optimized for performance and density with the development tools that are critical in the optimal mapping of designs.

Megafunctions provide total solutions by targeting specific application areas, providing optimized performance and system reusability, and significantly reducing a system's time-to-market.

Reducing a Designer's Time-to-Market

Altera recommends the use of ready-made, pretested functional blocks—called megafunctions—to augment existing hardware description language (HDL) design methodology. When implementing complex system architectures, these megafunctions significantly reduce design tasks, dramatically shorten design cycles, and leverage existing intellectual property.

By using megafunctions, designers can focus more time and energy on improving and differentiating their system-level product, rather than redesigning common off-the-shelf functions. Altera addresses this design need with megafunctions developed through the Altera Megafunction Partners Program (AMPP℠) and with Altera-created megafunctions, called MegaCore™ functions. Altera also provides free reference designs to help designers start the implementation process.



Contents

Altera Megafunction Partners Program

The Altera Megafunction Partners Program (AMPP), an alliance between Altera and developers of synthesizable megafunctions, brings the advantages of design reuse to users of Altera PLDs and provides product breadth to Altera's megafunction offering. Through this alliance, AMPP vendors develop megafunctions that are optimized for Altera devices.

MegaCore Functions

MegaCore functions are developed, pre-tested, documented, and licensed by Altera as MAX+PLUS® II migration products. These functions are optimized for a specific Altera device architecture, allowing user-specified performance utilization goals to be met. Altera MegaCore functions aid in critical design implementation and help reduce design tasks and development cycles.

Reference Designs

Altera reference designs provide entry-level solutions to help get designers started. Reference designs may include source code that can be easily modified to fit a designer's specific requirements.

MegaWizard Plug-Ins

Altera MegaWizard™ Plug-Ins allow designers to customize associated megafunctions with minimal effort and then integrate them into any design flow with any EDA tool. Both Altera and its AMPP partners are offering parameterized functions that the users control by linking MegaWizard Plug-Ins to their functions.

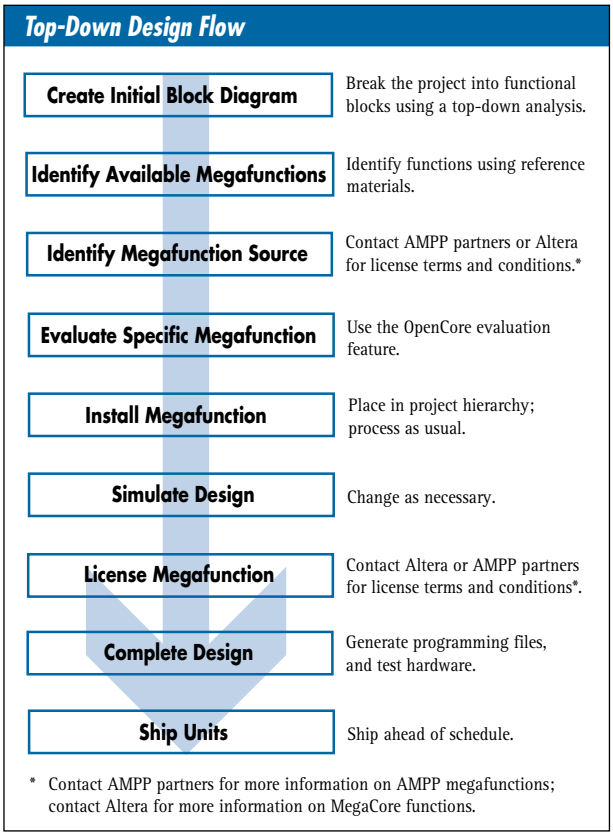
Designers using megafunctions powered by a MegaWizard Plug-In save time and money because they now handle customization efficiently in their own design environment.

OpenCore Feature

The Altera MAX+PLUS II software provides the OpenCore™ feature. OpenCore allows designers to instantiate, compile, and simulate a function to verify its size and performance before making a purchase decision.

Designing from the Top-Down

Having a project flow smoothly is critical for design success. The development process for megafunctions, shown in the chart below, helps guarantee success.



Increase Performance and Add Flexibility with FLEX DSP

Designers traditionally have been forced to make a tradeoff between the flexibility of DSP processors and the performance of DSP ASIC and ASSP solutions. FLEX DSP™ eliminates this tradeoff, providing both exceptional performance and the flexibility inherent to PLDs. This solution ranges from parameterized FIR filter reference designs to optimized higher-level FFT and adaptive FIR filter megafunctions.

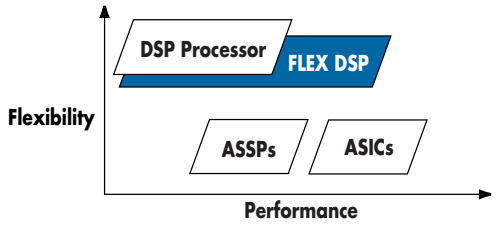
The Altera FLEX DSP solution provides optimized performance that is ideal for real-time, high-performance applications such as satellite communications, digital image processing, and spread-spectrum systems.

Altera's FLEX DSP solution includes:

- DSP building blocks such as FIR filters and high-speed multipliers
- DSP imaging functions for convolution, filtering, and compression
- DSP error control coding solutions such as Reed-Solomon and Viterbi CODECs
- DSP communication functions for wireless and broadband applications

The tables at the right show key performance benchmarks for high-speed multipliers implemented with the library of parameterized modules (LPM) function lpm_mult, and the FFT MegaCore function.

FLEX DSP Overview



Multiplier (lpm_mult) Performance

Size	Pipelined Performance	Logic Cells
8 x 8	179 MHz	145
16 x 16	109 MHz	561

FFT MegaCore Performance

Length (Points)	Precision	Memory	Logic Cells	Benchmark
512	8 Data 8 Twiddle	Dual, Internal	1,075	40.3 µsec
512	12 Data 12 Twiddle	Dual, Internal	2,058	65.5 µsec
1,024	16 Data 16 Twiddle	Dual, External	3,100	183 µsec
32K	16 Data 16 Twiddle	Dual, External	3,100	8,657 µsec

DSP Building Blocks

Altera's DSP building blocks include functions such as high-speed multipliers, floating-point arithmetic functions, IIR filters, and round/saturate functions. These parameterized functions are optimized for both performance and flexibility in Altera's FLEX® architectures, and can be combined to implement efficient DSP systems.

DSP Building Blocks

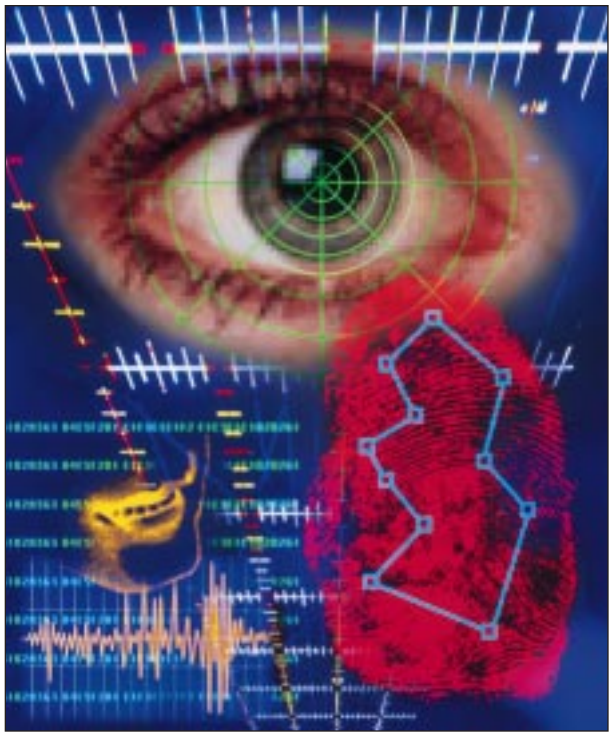
Function Description	Source	Product Family	Reference Document
Square Root Operator	Integrated Silicon Systems	FLEX	–
Floating-Point Adder	Integrated Silicon Systems	FLEX	–
Floating-Point Divider	Integrated Silicon Systems	FLEX	–
Floating-Point Multiplier	Integrated Silicon Systems	FLEX	–
Rank Order Filter Library	Integrated Silicon Systems	FLEX	–
Median Filter Library	Integrated Silicon Systems	FLEX	–
IIR Filter Library	Integrated Silicon Systems	FLEX 10K	M-SB-003-00
FIR Filter Library	Integrated Silicon Systems	FLEX	–
Parameterized Integer Divider	Integrated Silicon Systems	FLEX 10K	–
Parameterized Tap-Size Parallel FIR Filter	Altera Reference Design	FLEX	A-FS-01-01
Parameterized Tap-Size Serial FIR Filter	Altera Reference Design	FLEX	A-FS-01-01
Parameterized Floating-Point Adder/Subtractor	Altera Reference Design	FLEX	A-FS-02-01
Parameterized Integer Divider	Altera Reference Design	FLEX	A-FS-03-01
Parameterized Floating-Point Multiplier	Altera Reference Design	FLEX	A-FS-04-01
Data Word Rounder	Altera Reference Design	FLEX	A-FS-05-01
Data Word Saturator	Altera Reference Design	FLEX	A-FS-06-01

DSP Building Block Documentation

Document	Description	Reference Document
AN 73	Implementing FIR Filters in FLEX Devices	A-AN-073-01
AN 83	Binary Numbering Systems	A-AN-083-01
PIB 23	Digital Signal Processing in FLEX Devices	A-PIB-023-01
TB 3	FLEX Devices as Alternative to DSP ASSPs and DSP ASICs	M-TB-DSP1-01
TB 4	Using FLEX Devices as DSP Coprocessors	M-TB-DSP2-01
TB 5	Implementing Multipliers in FLEX 10K EABs	M-TB5-10KEAB-01
TB 12	FLEX 10K vs. FPGA Performance	M-TB-012-01
SB 3	Biquad IIR Filter Megafunction	A-SB-003-01
FS 1	FIR Filters	A-FS-01-01
FS 2	fp_add_sub Floating-Point Adder/Subtractor	A-FS-02-01
FS 3	Integer Dividers	A-FS-03-01
FS 4	fp_mult Floating-Point Multiplier	A-FS-04-01
FS 5	round Data Word Rounder	A-FS-05-01
FS 6	saturate Data Word Saturator	A-FS-06-01
Conference Paper	Enhancing Fixed-Point DSP Processor System Performance with PLDs as a DSP Coprocessor	1997 Design SuperCon Proceedings
Conference Paper	DSP Processor Architecture for Programmable Logic	1997 ICSPAT Proceedings
Conference Paper	DSP Implementation in Programmable Logic	1996 IEEE VLSI Conference
Conference Paper	DSP Building Blocks in Programmable Logic	1997 DSP World Proceedings
News Article	DSP Tools in Programmable Logic: A Look Ahead	May 1997 Computer Design
News Article	DSP Megafunctions in Programmable Logic Optimize Performance and Shrink Design Cycles	March 1997 EE Times

DSP Imaging Solutions for Complex Applications

DSP imaging solutions from Altera provide functional blocks for convolution, compression, and filtering applications. Compression support includes discrete cosine transform and JPEG megafunctions that are optimized with the memory structure of the FLEX 10K embedded array block. Filtering megafunctions that support imaging applications include decimating and biorthogonal wavelet filters.



DSP Error Control Coding (ECC) Solutions

ECC is a methodology that detects, and in some cases, corrects errors induced in digital data during transmission over a noisy channel (digital video/audio broadcast) or during storage in an unreliable medium (e.g., compact disc, digital tape). Coding types, including Reed Solomon and Viterbi, detect and correct these errors.

DSP Imaging

Function Description	Source	Product Family	Reference Document
Parameterized Discrete Cosine Transform	Integrated Silicon Systems	FLEX 10K	A-SB-09-01
Image Processing Library	Integrated Silicon Systems	FLEX 10K	–
JPEG Decoder/Encoder	Integrated Silicon Systems	FLEX 10K	–
Parameterized Decimating Filter	FASTMAN	FLEX 10K, FLEX 8000	A-SB-014-01
Biorthogonal Wavelet Filter	FASTMAN	FLEX 10K	A-SB-015-01
RGB2YCrCb/YCrCb2RGB Color Space Converters	Altera MegaCore Function	FLEX	A-DS-RGB-01/A-SB-027-01

DSP Imaging Documentation

Document	Description	Reference Document
AN 82	Highly Optimized 2-D Convolvers in FLEX 10K Devices	A-AN-082-01
TB 8	Implementing Multirate Filters in FLEX Devices	M-TB8-DSP3-01
SB 9	Discrete Cosine Transform Megafunction	A-SB-009-01
SB 14	Decimating Filter Megafunctions	A-SB-014-01
SB 15	Biorthogonal Wavelet Filter Megafunction	A-SB-015-01
Data Sheet	RGB2YCrCb and YCrCb2RGB Color Space Converters	A-DS-RGB-01

DSP Error Control Coding Solutions

Function Description	Source	Product Family	Reference Document
Viterbi Decoder	CAST	FLEX 10K, FLEX 6000	–
Parameterizable Reed-Solomon Encoder/Decoder	HammerCores	FLEX	–
Reed Solomon Decoder/Encoder	Integrated Silicon Systems	FLEX 10K	–
Viterbi Decoder	Integrated Silicon Systems	FLEX 10K	–
Trellis Coded Modulation (TCM) Decoder/Encoder	Integrated Silicon Systems	FLEX 10K	–
Convolutional Encoder	Integrated Silicon Systems	FLEX 10K	–
Intermediate Data Rate (IDR) Framer/Deframer	Integrated Silicon Systems	FLEX 10K	–
CRC Checker/Generator	Altera MegaCore Function	FLEX 10K	A-DS-CRC-01

Wireless and Broadband Communications

The DSP communications solution supports wireless and broadband applications. The building blocks for these applications include functions ranging from numerically controlled oscillators (NCOs) and complex mixers to linear feedback shift registers (LFSRs), digital modulators, and FFT functions. The functions are integrated to complete system-level solutions. Target applications for these solutions include cellular basestations, PCS, ADSL, and cable modems.

DSP Wireless and Broadband Communications

Function Description	Source	Product Family	Reference Document
Adaptive Equilizer	HammerCores	FLEX	–
Adaptive Filter	Integrated Silicon Systems	FLEX 10K	A-SB-002-01
Fast Fourier Transform (FFT)/IFFT	Integrated Silicon Systems	FLEX 10K	–
Adaptive Equalizer	Integrated Silicon Systems	FLEX 10K	–
Block and Convolutional Interleavers/Deinterleavers	Integrated Silicon Systems	FLEX 10K	–
Convolutional Interleaver (Cable Modem and PCS)	KTech Telecommunications	FLEX, MAX 9000	A-SB-016-01
Telephony Tone Generation	NComm	FLEX 10K	–
Complex Mixer/Multiplier	Nova Engineering	FLEX	A-SB-004-01
Numerically Controlled Oscillator	Nova Engineering	FLEX 10K	A-SB-005-01
Digital Modulator	Nova Engineering	FLEX 10K	A-SB-010-01
Linear Feedback Shift Register	Nova Engineering	FLEX, MAX 9000	A-SB-011-01
Early/Late Gate Symbol Synchronizer	Nova Engineering	FLEX, MAX 9000	A-SB-017-01
Binary Pattern Correlator	Nova Engineering	FLEX, MAX 9000	A-SB-018-01
Fast Fourier Transform	Altera MegaCore Function	FLEX 10K	A-SB-012-01/A-DS-FFT-03
FFT-on-Chip	Altera Reference Design	FLEX	A-AN-084-02/A-FS-07-01

DSP Wireless and Broadband Communications Documentation

Document	Description	Reference Document
AN 84	Implementing FFT with On-Chip RAM in FLEX 10K Devices	A-AN-084-02
SB 2	High-Speed Adaptive FIR Filter Megafunction	A-SB-002-01
SB 4	Complex Multiplier/Mixer Megafunction	A-SB-004-01
SB 5	Numerically Controlled Oscillator Megafunction	A-SB-005-02
SB 10	Digital Modulator Megafunction	A-SB-010-01
SB 11	Linear Feedback Shift Register Megafunction	A-SB-011-01
SB 12	Fast Fourier Transform MegaCore Function	A-SB-012-01
SB 16	Convolutional Interleaver Megafunction	A-SB-016-01
SB 17	Binary Correlator Megafunction	A-SB-017-01
SB 18	Early/Late Gate Symbol Synchronizer Megafunction	A-SB-018-01
FS 7	FFT-on-Chip Fast Fourier Transform	A-FS-07-01
Data Sheet	FFT Fast Fourier Transform	A-DS-FFT-03
Conference Paper	Automated Design Tools for Adaptive Filter Development	DSP Scandinavia 1996 Proceedings
Conference Paper	Automated FFT Processor Design	1996 ICSPAT Proceedings
Conference Paper	PLD-Based FFTs	1997 ICSPAT Proceedings
Conference Paper	A PLD-Based Solution for Cable Modem	1997 ICSPAT Proceedings
Conference Paper	Parameterizable Reed-Solomon CODECs	1998 DSP Spring Proceedings
Conference Paper	Pipelined Adaptive Filters in PLDS	1997 ICSPAT Proceedings

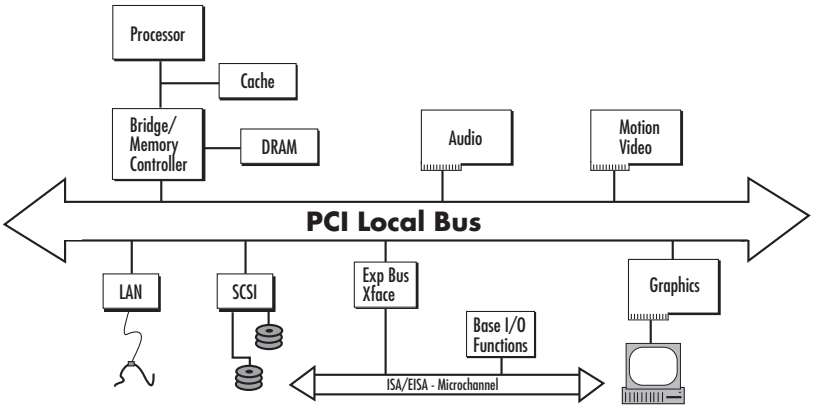
Bus Interfaces: Megafunctions Create Easy-to-Use Peripherals

Bus interface solutions support peripheral component interconnect (PCI), universal serial bus (USB), controller area network (CAN) bus, inter-integrated circuit (IIC) bus, and the IEEE 1394 serial bus. These solutions enable designers to focus on differentiating elements of the design, typically the local bus interface and the custom configurable logic.

Custom Interconnecting with PCI

The peripheral component interconnect (PCI) bus serves as a device-level interconnect for peripherals on a circuit board, and as a bus for high-performance expansion cards. The PCI bus architecture is ideal for applications such as network adapters, storage and embedded controllers, graphic accelerator boards, and audio-video products. Altera FLEX 10K, FLEX 8000, FLEX 6000, MAX® 9000, and MAX 7000 devices provide a programmable logic solution for a variety of PCI applications. PCI megafunctions include 32-bit target and 32-bit master/target functions.

The figure below shows a typical PCI local bus system architecture and does not imply any specific architectural limits. In this example, the processor/cache/memory sub-system is connected to a PCI bus through a PCI bridge.



The Altera solution provides critical advantages for the system designer. Altera's high-density FLEX devices enable a designer to create a single-device solution that includes both the PCI interface and the application-specific logic for a custom solution. Altera's PCI megafunctions deliver compliance and optimization, and significantly reduce design efforts.

Easier-to-Use Peripherals with USB

The universal serial bus (USB) megafunctions, provided by the AMPP program, are key tools in developing easier-to-use peripherals. In the past, PC peripheral devices required their own ports and forced the user to open the case and insert a board, which often involved difficult configuration schemes. With USB, users can expect a low-cost, flexible solution supporting out-of-system PC connections with no difficult configuration schemes.

Optimized Megafunctions with CAN

The controller area network (CAN) bus megafunction, provided by the AMPP program, is ideal for applications including automotive electronics, home automation, and simple sensor/actuator systems.

Total Control with IIC Bus Interfaces

The inter-integrated circuit (IIC) bus interface is a general-purpose interface used to connect several peripheral devices to one controlling unit. The interface can support active devices with different clock domains. IIC interface allows a device other than a CPU to be defined as the master on the IIC bus, providing a key advatange to the designer. IIC megafunctions, provided by the AMPP program, include both master and slave functions.

Increased Versatility with IEEE 1394

The IEEE 1394 serial bus is a connectivity standard for versatile, high-speed multimedia applications in the PC and consumer electronics markets. IEEE 1394 uses a single industry-standard connector cable, eliminating complications and improving ease-of-use and economies of scale. IEEE 1394 is ideal for applications such as multimedia and PC/peripherals, set-top boxes, digital camcorders, HDTV, and digital cameras.

Bus Interface Megafunctions

Function Description	Source	Product Family	Reference Document
32-Bit PCI Target with Burst	Eureka Technology	FLEX 10K, FLEX 8000	A-SB-006-01
32-Bit PCI Master/Target with Burst	Eureka Technology	FLEX, MAX	A-SB-019-01
32-Bit PCI Target	PLD Applications	FLEX	A-SB-025-02
32-Bit PCI Master/Target with Burst	PLD Applications	FLEX 10K, FLEX 6000	A-SB-026-02
32-Bit PCI Target with Burst	Altera MegaCore	FLEX	A-DS-PCI2-01
32-Bit PCI Master/Target with Burst	Altera MegaCore	FLEX	A-DS-PCI1-02/A-SB-020-01
IIC Master/Slave	SICAN Microelectronics	FLEX	A-SB-031-01
CAN Bus	SICAN Microelectronics	FLEX	A-SB-022-01
IEEE 1394 Firewire	SIS Microelectronics	FLEX 10K	–
1394A Core	Phoenix Technologies	FLEX 10K	–
USB Function Controller	Sapien Design	FLEX 10K, FLEX 8000	A-SB-024-01
USB Host Controller	Sapien Design	FLEX 10K, FLEX 8000	A-SB-028-01

Bus Interface Documentation

Document	Description	Reference Document
AN 41	PCI Bus Applications for Altera Devices	A-AN-041-01
AN 86	Implementing the PCI/A Master/Target	A-AN-086-01
AB 140	PCI Compliance of Altera Devices	A-AB-140-01
SB 6	PCI Bus Target Megafunction	A-SB-006-01
SB 19	PCI Bus Master/Target Megafunction	A-SB-019-01
SB 20	PCI Master/Target MegaCore Function	A-SB-020-01
SB 22	CAN Bus Megafunction	A-SB-022-01
SB 24	USB Function Controller Megafunction	A-SB-024-01
SB 25	PLDA PCI Bus Target Interface Megafunction	A-SB-025-01
SB 26	PLDA PCI Master/Target Interface Megafunction	A-SB-026-01
SB 28	USB Host Controller Megafunction	A-SB-028-01
SB 31	IIC Interface Megafunctions	A-SB-031-01
TB 26	FLEX 10K and PCI/A: The Complete PCI Solution	M-TB-026-01
Data Sheet	PCI Master/Target MegaCore Function with DMA Data Sheet	A-DS-PCI1-02
Data Sheet	PCI Target MegaCore Function with DMA Data Sheet	A-DS-PCI2-02
Conference Paper	Using a Design Foundation for Flexible and Rapid PCI Interface Dev.	PCI Spring 1996 Proceedings
Conference Paper	A VHDL Design Approach to a Master/Target PCI Interface	PCI Spring 1996 Proceedings
Conference Paper	Programmable Logic Devices in a Switched PCI Bus System	1997 PCI Plus Proceedings
Customer Application	Bailey Controls Uses Megafunctions to Solve the PCI Challenge	M-CAS-BCCO-01

Processor and Peripheral Megafunctions

Processor and peripheral megafunctions focus on providing solutions for microcontrollers, embedded processors, CPU cores, and peripheral functions such as UARTs and interrupt controllers. These solutions enable designers to focus on differentiating elements of the design and use their existing building blocks to architect systems ranging from interface line cards to communication systems.

Processor and Peripheral Megafunctions

Function Description	Source	Product Family	Reference Document
C_UART	CAST	FLEX and MAX	–
C 8251 Programmable Communication Interface	CAST	FLEX	–
AC6850 ACIA	CAST	FLEX and MAX	–
C29116A Programmable Peripheral Interface	CAST	FLEX 10K	–
C2910/C2910A Microprogram Controller	CAST	FLEX	–
C49410 Microprogram Controller	CAST	FLEX	–
C8051 Microcontroller	CAST	FLEX 10K	–
C8255A Programmable Peripheral Interface	CAST	FLEX and MAX	–
XMIDI Modules UART Library	DDD	FLEX and MAX	–
XM-01 XMIDI Basic UART	DDD	FLEX and MAX	–
IEEE 1284 Parallel Slave Interface	SIS Microelectronics	FLEX	–
RAW8051-A	RWA	FLEX 10K	–
RAW8052-A	RWA	FLEX 10K	–
BareCore 8052-A	RWA	FLEX 10K	–
V6502 Microprocessor	VAutomation	FLEX 10K	–
VZ80 Microprocessor	VAutomation	FLEX 10K	–
A8251A Communication Interface	Altera MegaCore Function	FLEX 10K, FLEX 8000	A-DS-A8251-01
A6402 UART	Altera MegaCore Function	FLEX and MAX	A-DS-A6402-01
A16450 UART	Altera MegaCore Function	FLEX and MAX	A-DS-A16450-01
A6850 ACIA	Altera MegaCore Function	FLEX and MAX	A-DS-A6850-01
A8237 DMA Controller	Altera MegaCore Function	FLEX	A-DS-A8237-01
A8255 Programmable Peripheral Interface Adapter	Altera MegaCore Function	FLEX and MAX	A-DS-A8255-01
A8259 Programmable Interrupt Controller	Altera MegaCore Function	FLEX and MAX	A-SB-021-01/A-DS-A8259-01

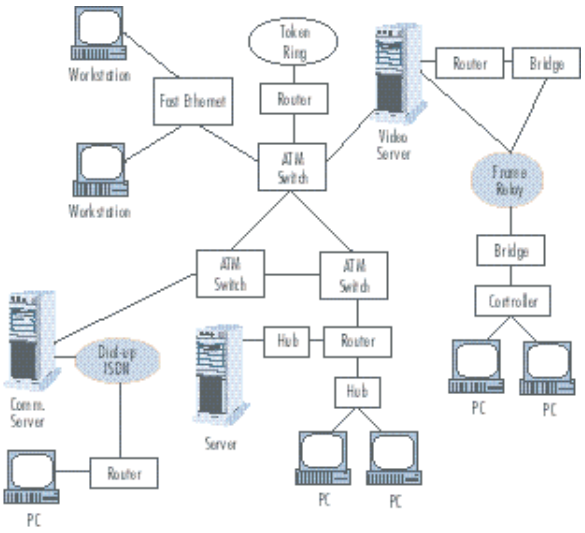
Processor and Peripheral Documentation

Document	Description	Reference Document
SB 21	A8259 MegaCore Function	A-SB-021-01
SB 23	Microperipheral MegaCore Library	A-SB-023-01
Data Sheet	a8251 Programmable Communications Interface MegaCore Function	A-DS-A8251-01
Data Sheet	a6402 UART MegaCore Function	A-DS-A6402-01
Data Sheet	a16450 UART MegaCore Function	A-DS-A16450-01
Data Sheet	a6850 Asynchronous Communications Interface MegaCore Function	A-DS-A6850-01
Data Sheet	A8237 DMA Controller	A-DS-A8237-01
Data Sheet	A8255 Programmable Peripheral Interface Adapter	A-DS-A8255-01
Data Sheet	A8259 Programmable Interrupt Controller	A-SB-021-01/A-DS-A8259-01

Networking Megafunctions

Networking solutions are aimed at providing megafunctions in telecommunication and data communication target applications. These building blocks enable designers to architect systems ranging from interface line cards to serial communication systems.

This communications solution includes a CRC library, ATM functions, an HDLC controller, and an ADPCM transcoder. The figure at the right shows a typical topology of interconnecting network.



Networking Megafunctions			
Function Description	**Source**	**Product Family**	**Reference Document**
Speedbridge Speed-Matching FIFO	SIS Microelectronics	FLEX 10K, FLEX 8000	A-SB-013-01
High-Level Data Link Controller (HDLC) Protocol Core	Integrated Silicon Systems	FLEX 10K	–
ADPCM Transcoder G.721/723/726/727 Compliant	Integrated Silicon Systems	FLEX 10K	A-SB-008-01
CRC Checker/Generator	Altera MegaCore Function	FLEX	A-DS-CRC-01/A-SB-030-01

Networking Megafunctions Documentation		
Document	**Description**	**Reference Document**
SB 8	ADPCM Megafunction	A-SB-008-01
SB 13	Speedbridge Megafunction	A-SB-013-01
SB 30	CRC MegaCore Function Parameterized CRC Generator/Checker	A-SB-030-01
Data Sheet	CRC MegaCore Function	A-DS-CRC-01
Conference Paper	MegaFunctions for PLD-Based Telecommunications Products	1998 DesignCon Proceedings

Visit the Altera World-Wide Web Site

Altera provides additional reference documentation including an AMPP catalog and a Microperipheral MegaCore Library Data Book. For the latest literature, information on Altera, and Megafunctions updates, go to the Altera world-wide web-site at http://www.altera.com.

Additional Documentation		
Type	**Description**	**Reference Document**
Catalog	AMPP Catalog	M-CAT-AMPP-02
Data Book	Microperipheral MegaCore Library Data Book	A-DB-MEGA-02

ALTERA MEGAFUNCTION PARTNERS PROGRAM

AMPP Partners Directory

For a complete list of AMPP partners, consult the Altera AMPP Catalog or the Altera world-wide web site at **http://www.altera.com.**

CAST
Expertise: Peripherals & DSP
24 White Birch Drive
Pomona, NY 10970
Telephone: [914] 354-4945
Email: info@cast-inc.com

Digital Design & Development
Expertise: Peripherals
18A Godshuis Street, 1861
Meise, Belgium
Telephone: [32] 2-270-2797
Email:
73261.530@compuserve.com

Eureka Technology
Expertise: Bus Interfaces
4962 El Camino Real, Suite 108
Los Altos, CA 94022
Telephone: [415] 960-3800
Email: info@eurekatech.com

FASTMAN
Expertise: DSP
1613 Capitol of Texas Hwy. S.
Suite 222
Austin, TX 78746
Telephone: [512] 328-9088
Email: mrt@fastman.com

HammerCores
Expertise: DSP & Networking
http://www.hammercores.com

Integrated Silicon Systems
Expertise: DSP and Networking
50 Malone Road
Belfast, BT9 5BS
Northern Ireland
Telephone: [44] 1232-664-664
Email: info@iss-dsp.com

KTech Telecommunications
Expertise: Wireless
15501 San Fernando–
Mission Blvd.
Suite 100
Mission Hills, CA 91345
Telephone: [818] 361-2248
Email: skuh@ktechtelecom.com

NComm
Expertise: Networking
401 Main Street
Suite 204
Salem, New Hampshire 03079
Telephone: [603] 893-6186
Email: info.ncomm.com

Nova Engineering
Expertise: DSP
5 Circle Freeway Drive
Cincinnati, OH 45246-1105
Telephone: [513] 860-3456
Email: info@nova-eng.com

PLD Applications
Expertise: Bus Interfaces
14 Rue Soleillet
75971 Paris Cedex 20
Telephone: [33] 1 40 33 79 98
Email: plda@worldnet.fr

Pheonix Technologies
Expertise: Bus Interfaces
411 E. Plumeria Drive
San Jose, CA 95136
Telephone: [408] 570-1000
Email: sales@vchips.com

Richard Watts Associates
Expertise: Processors
8 Church Square
Leighton Buzzard, Bedfordshire
LU7 7AE
England, UK
Telephone: [44] 01525 372621
Email:
coreinfo@evolution.co.uk

Sapien Design
Expertise: Bus Interfaces
45335 Potawatami Drive
Fremont, CA 94539
Telephone: [510] 668-0200
Email: sapien@pacbell.net

SICAN Microelectronics
Expertise: Bus Interfaces
400 Oyster Point Blvd.
Suite 512
S. San Francisco, CA 94080
Telephone: [415] 871-1494
Email:
ampp@SICAN-micro.com

SIS Microelectronics
Expertise: Networking
1831 LeftHand Circle, Suite E
P.O. Box 1432
Longmont, CO 80501
Telephone:
[303] 776-1667 x223
Email: info@sismicro.com

VAutomation
Expertise: Processors
20 Trafalgar Square
Nashua, NH 03063
Telephone: [603] 882-2282
Email:
ampp@VAutomation.com

Altera Offices

Altera Corporation
101 Innovation Drive
San Jose, CA 95134
Telephone: (408) 544-7000
http://www.altera.com

Altera European Headquarters
Holmers Farm Way
High Wycombe
Buckinghamshire
HP12 4XF
United Kingdom
Telephone: (44) 1 494 602 000

Altera Japan Ltd.
Shinjuku Mitsui Bldg. 36F
1-1, Nishi-Shinjuku, 2 Chome
Shinjuku-ku, Tokyo 163-0436
Japan
Telephone: (81) 3 3340 9480

Altera International Ltd.
Suites 908-920, Tower 1
MetroPlaza
223 Hing Fong Road
Kwai Fong, New Territories
Hong Kong
Telephone: (852) 2487 2030

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