In-System Programmability Selector Guide

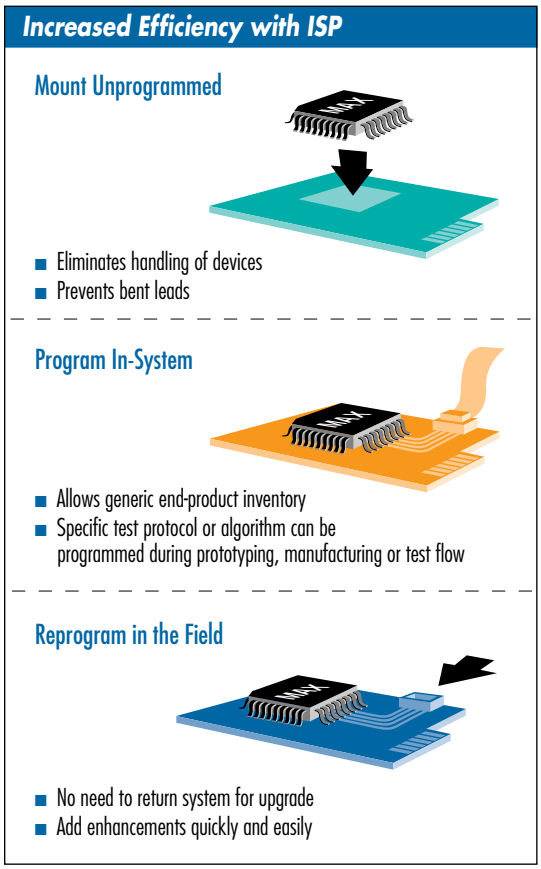
April 1997

In-System Programmability (ISP) Provides Maximum Flexibility

Altera's in-system programmability (ISP) allows for easy prototyping during design development, streamlines the manufacturing flow process, and adds significant flexibility, for even the most complex of designs. Quick and efficient field upgrades are also a breeze with Altera's ISP.

Whether a customer is using the Altera ByteBlaster™ cable during prototyping, automatic test equipment (ATE) during manufacturing, or an embedded processor for field upgrades, Altera's ISP-based products and support provide an industry-standard solution for all types of applications.

Available in both MAX® 9000 and MAX 7000S devices, the ISP feature uses the industry-standard Joint Test Action Group (JTAG) test ports. This interface allows devices to be programmed and the printed circuit board to be functionally tested in a single manufacturing step, saving testing times and assembly costs.



MAX 9000 and MAX 7000S devices provide an industry-standard, four-pin JTAG ISP interface for programming a device after it has been mounted onto a printed circuit board.

MAX 9000 Devices

The high-density MAX 9000 products, which includes the original MAX 9000 devices and the new higher-speed MAX 9000A devices, provide innovative solutions for today's design challenges. By offering a wide variety of advanced system-level features—such as ISP, built-in JTAG boundary-scan test support, and MultiVolt™ I/O capability—the MAX 9000 family addresses these design challenges at the device level.

The MAX 9000 family builds on the success of Altera's popular MAX 7000 family, while offering higher densities and maintaining the industry's highest performance. Ranging from 320 to 560 macrocells (6,000 to 12,000 usable gates), the MAX 9000 family has propagation delays from 7.5 to 20 ns and typical in-system performance of 50 MHz. In addition, the devices in each MAX 9000 package type are function- and pin-compatible. This compatibility makes it easy to migrate designs from one density level to another while maintaining pin assignments, which eliminates the need for board layout changes.

MAX 9000 Highlights

FEATURE	BENEFIT
ISP	Easy prototyping In-field upgrades Simplifies manufacturing flow
6,000 to 12,000 usable gates 320 to 560 macrocells	Improves system integration Ideal for gate-array prototyping
7.5-ns propagation delays	Increase in-system performance to 133 MHz
MultiVolt I/O operation	Ideal for mixed-voltage systems
Built-in JTAG support	Simplifies device and system testing

MAX 9000 Devices					
DEVICE	MACRO-CELLS	PIN/PACKAGE OPTIONS	I/O PINS[1]	TEMP.	SPEED GRADE
EPM9320	320	84-Pin PLCC, 208-Pin RQFP, 280-Pin PGA, 356-Pin BGA	60, 132, 168	C	-15
	320	84-Pin PLCC, 208-Pin RQFP, 280-Pin PGA, 356-Pin BGA	60, 132, 168	C, I	-20
EPM9320A	320	84-Pin PLCC, 208-Pin RQFP, 356-Pin BGA	60, 132, 168	C	-7, -10
	320	84-Pin PLCC, 208-Pin RQFP, 356-Pin BGA	60, 132, 168	C, I	-15
EPM9400	400	84-Pin PLCC, 208-Pin RQFP, 240-Pin RQFP	59, 139, 159	C	-15, -20
EPM9400A	400	84-Pin PLCC, 208-Pin RQFP, 240-Pin RQFP	59, 139, 159	C	-10, -12
	400	84-Pin PLCC, 208-Pin RQFP, 240-Pin RQFP	59, 139, 159	C, I	-15
EPM9480	480	208-Pin RQFP, 240-Pin RQFP	146, 175	C	-15, -20
EPM9480A	480	208-Pin RQFP, 240-Pin RQFP	146, 175	C	-10, -12
	480	208-Pin RQFP, 240-Pin RQFP	146, 175	C, I	-15
EPM9560	560	208-Pin RQFP, 240-Pin RQFP, 280-Pin PGA, 304-Pin RQFP, 356-Pin BGA	153, 191, 216	C	-15
	560	208-Pin RQFP, 240-Pin RQFP, 280-Pin PGA, 304-Pin RQFP, 356-Pin BGA	153, 191, 216	C,I	-20
EPM9560A	560	208-Pin RQFP, 240-Pin RQFP, 304-Pin RQFP, 356-Pin BGA	153, 191, 216	C	-10, -12
	560	208-Pin RQFP, 240-Pin RQFP, 304-Pin RQFP, 356-Pin BGA	153, 191, 216	C,I	-15

Notes: [1] Four I/O pins are dedicated inputs.

MAX 7000S Devices

Ranging from 32 to 256 macrocells (600 to 5,000 usable gates), MAX 7000S devices are ideal for system-level integration. Altera's MAX 7000S devices feature ISP, and devices with 128 or more macrocells have built-in JTAG boundary-scan test circuitry. The enhanced MAX 7000S devices feature six output enable signals, two global clocks, fast input registers, and programmable slew-rate control.

MAX 7000S Highlights	
FEATURE	BENEFIT
ISP	Easy prototyping In-field upgrades Simplifies manufacturing flow
600 to 5,000 usable gates	Multiple density options
32-macrocell, 44-pin devices to 256-macrocell, 208-pin devices	High pin-to-logic ratios for a wide variety of applications
5-ns propagation delays	Provide over 175-MHz counter frequencies
Built-in JTAG support	Simplifies device and system testing
Clock multiplier	Improves system performance, bandwidth, and area efficiency
Programmable power-saving mode	Enables greater than 50% power reduction
MultiVolt I/O operation	Ideal for mixed-voltage systems
PCI compliance	Satisfies PCI bus requirements

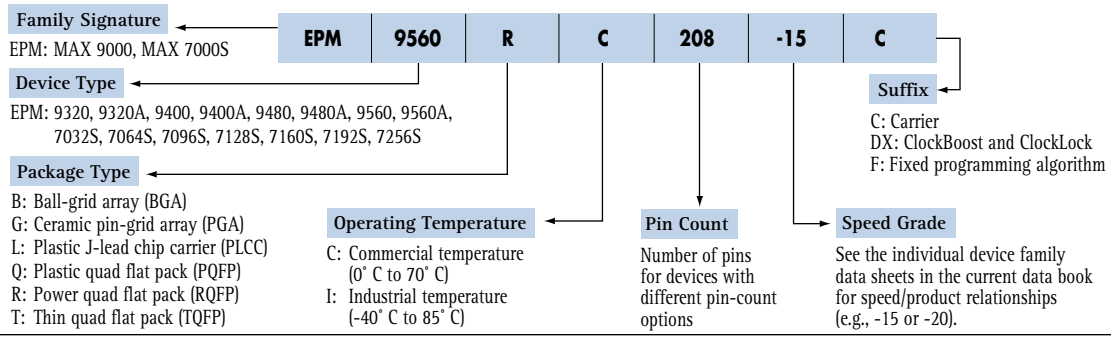
These enhanced features enable MAX 7000S devices to address a broad range of system-level applications. For example, the six logic- or pin-controlled output enable signals allow direct connection to multiple buses found in microprocessor-controlled systems. The two high-speed global clocks provide increased flexibility. The fast setup times enable high-speed, device-to-device communication. For even faster on-chip performance, MAX 7000S device options incorporate on-chip clock multiplier circuitry that enhances bandwidth and overall system performance.

Finally, the programmable output slew-rate control helps reduce system noise by slowing the switching time of non-speed-critical outputs. A programmable power-saving feature allows for 50% or greater power reduction in each macrocell.

MAX 7000S Devices

DEVICE	MACRO-CELLS	PIN/PACKAGE OPTIONS	I/O PINS	TEMP.	SPEED GRADE	t_{PD} (ns)	f_{CNT} (MHz)
EPM7032S	32	44-Pin PLCC/TQFP	36	C	-5	5	178.6
	32	44-Pin PLCC/TQFP	36	C	-6	6	150
	32	44-Pin PLCC/TQFP	36	C	-7	7.5	125
	32	44-Pin PLCC/TQFP	36	C, I	-10	10	100
EPM7064S	64	44-Pin PLCC/TQFP, 84-Pin PLCC, 100-Pin TQFP	36, 52, 68	C	-6	6	150
	64	44-Pin PLCC/TQFP, 84-Pin PLCC, 100-Pin TQFP	36, 52, 68	C	-7	7.5	125
	64	44-Pin PLCC/TQFP, 84-Pin PLCC, 100-Pin TQFP	36, 52, 68	C, I	-10	10	100
EPM7096S	96	84-Pin PLCC, 100-Pin TQFP	52, 64, 76	C	-6	6	150
	96	84-Pin PLCC, 100-Pin TQFP	52, 64, 76	C	-7	7.5	125
	96	84-Pin PLCC, 100-Pin TQFP	52, 64, 76	C, I	-10	10	100
EPM7128S	128	84-Pin PLCC, 100-Pin PQFP/TQFP, 160-Pin PQFP	68, 84, 100	C	-6	6	150
	128	84-Pin PLCC, 100-Pin PQFP/TQFP, 160-Pin PQFP	68, 84, 100	C	-7	7.5	125
	128	84-Pin PLCC, 100-Pin PQFP/TQFP, 160-Pin PQFP	68, 84, 100	C	-10	10	100
	128	84-Pin PLCC, 100-Pin PQFP/TQFP, 160-Pin PQFP	68, 84, 100	C, I	-15	15	76.9
EPM7160S	160	84-Pin PLCC, 100-Pin TQFP, 160-Pin PQFP	64, 84, 104	C	-7	7.5	125
	160	84-Pin PLCC, 100-Pin TQFP, 160-Pin PQFP	64, 84, 104	C	-10	10	100
	160	84-Pin PLCC, 100-Pin TQFP, 160-Pin PQFP	64, 84, 104	C, I	-15	15	76.9
EPM7192S	192	160-Pin PQFP	124	C	-7	7.5	125
	192	160-Pin PQFP	124	C	-10	10	100
	192	160-Pin PQFP	124	C, I	-15	15	76.9
EPM7256S	256	208-Pin RQFP/PQFP	132, 164	C	-7	7.5	125
	256	208-Pin RQFP/PQFP	132, 164	C	-10	10	100
	256	208-Pin RQFP/PQFP	132, 164	C	-12	12	90.9
	256	208-Pin RQFP/PQFP	132, 164	C, I	-15	15	76.9

Product Ordering Information



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