ALTERA®

Development Tools Selector Guide

July 1998

Introducing Altera Programmable Logic Development Tools

Altera offers the fastest, most powerful, and most flexible programmable logic development software and programming hardware in the industry. The Altera MAX+PLUS® II development tools provide a broad range of features with an easy-to-use graphical user interface. The MAX+PLUS II software also offers interfaces to industry-standard EDA tools that allow easy integration with your chosen design environment.

Altera development tools include the following features:

- Support for multiple device architectures, including the Altera FLEX® 10K, FLEX 6000, FLEX 8000, MAX® 9000, MAX 7000, MAX 5000, and Classic™ programmable logic device (PLD) families.
- Multi-platform support, including Microsoft Windows 95 and 98, and Windows NT for PCs, as well as X-Windows for Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations.
- Support for hardware description languages, including the VHDL 1987 and 1993 standards, Verilog HDL, and the Altera Hardware Description Language (AHDL).
- Interfaces to EDA tools that utilize EDIF 2 0 0 and 3 0 0 netlists, the library of parameterized modules (LPM), Standard Delay Format Files (**.sdf**), Verilog HDL, and VHDL.

Choosing the Right Tools for You

This development tools selector guide will help you choose the Altera MAX+PLUS II design environment that best meets your needs. The MAX+PLUS II design environment consists of the following elements:

- Design site and migration products
- MegaCore™ functions
- Maintenance support
- Programming hardware

At the end of this guide, you will find a list of recommended system configurations for all platforms supported by the MAX+PLUS II software, as well as descriptions of Altera's Commitment to Cooperative Engineering Solutions (ACCESS℠) program, Altera Megafunction Partners Program (AMPP℠) alliance, and Altera Consultants Alliance Program (ACAP℠).

Step 1 – Select a Design Site & Migration Products

You can configure your MAX+PLUS II development environment to suit your needs by combining a design site with migration product(s).

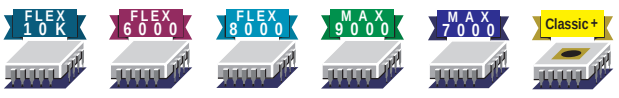
Your Altera design environment begins with a design site, which is identified with a **PLS** ordering code prefix (e.g., **PLS-BASE**). The design site offers the basic features and device support for designing with Altera PLDs.

You can obtain additional device support and features by ordering migration products, which are identified with a **PLSM** ordering code prefix (e.g., **PLSM-10K**). Migration products allow you to customize your MAX+PLUS II design environment by adding features to your design site. You can add migration products to your system at any time as your design needs change or expand.

Your choice of design site and migration products are determined by the following criteria:

Device Architecture Support

Altera supports the following device architectures:



The specific devices supported by each architecture are shown in the following table:

Device Architectures	Devices Supported
FLEX 10K	FLEX 10K, FLEX 10KE, FLEX 10KA
FLEX 6000	FLEX 6000, FLEX 6000A
FLEX 8000	FLEX 8000A
MAX 9000	MAX 9000, MAX 9000A
MAX 7000	MAX 7000, MAX 7000S, MAX 7000A
Classic+Plus	Classic and MAX 5000 families, EPF6010A, EPF6016, EPF6016A, EPF8282A, EPF8452A, EPM9320, EPM9320A, EPF10K10, and EPF10K10A devices

For detailed information on Altera devices, refer to the Altera Component Selector Guide, the current Altera data book, or the Altera world-wide web site at **http://www.altera.com**.

Software Features

MAX+PLUS II offers a wide variety of design entry, compilation, verification, programming, and other software features.

The Altera MAX+PLUS II Development Tools selection matrix on the following page shows which devices and software features are offered with each Altera product. From the matrix, choose one design site and as many migration products as you need for your design.

Altera MAX+PLUS II Development Tools

	Devices & Features Supported:	PC								UNIX Workstation			Notes
		PLS-BASE	PLS-MAGNUM	PLS-NET/PC	PLSM-ADE	PLSM-9K	PLSM-6K/8K	PLSM-10K	MegaCore Functions*	PLS-NXS/SN	PLS-NXS/HP	PLS-NXS/IBMRS	MegaCore Functions*	
Device Support	FLEX 10K		●	●				●		●	●	●		High-density, high-performance device family featuring embedded array blocks (EABs).
	FLEX 6000		●	●			●			●	●	●		Low-cost, high-performance alternative to gate arrays.
	FLEX 8000		●	●			●			●	●	●		High-performance Flexible Logic Element MatriX (FLEX) architecture device family.
	MAX 9000		●	●		●				●	●	●		High-density Multiple Array MatriX (MAX) architecture device family.
	MAX 7000	●	●	●						●	●	●		Second-generation MAX architecture that supports in-system programmability (ISP).
	Classic+Plus	●	●	●						●	●	●		For specific devices supported, refer to the device architecture support table on page 2.
Design Entry	Schematic Design Entry	●	●	●						●	●	●		The Graphic Editor and Symbol Editor provide basic building blocks for creating a design, including the library of parametrized modules (LPM), TTL, and custom functions.
	Text-Based Design Entry: AHDL and VHDL or Verilog HDL	●	●	●						●	●	●		MAX+PLUS II supports a high-level design methodology based on a variety of HDLs, including the Altera Hardware Description Language (AHDL), VHDL, and Verilog HDL.
	Waveform Design Entry		●	●	●					●	●	●		The Waveform Editor is used to specify logic by entering input and output waveforms.
	EDA Interfaces	●	●	●						●	●	●		The bidirectional EDIF interface and the VHDL and Verilog HDL netlist writers allow designers to import and export design files between MAX+PLUS II and industry-standard EDA tools.
	Floorplan Editing	●	●	●						●	●	●		The Floorplan Editor provides a graphical method for assigning logic cells and pins.
	Hierarchical Design Management	●	●	●						●	●	●		The Hierarchy Display allows you to easily traverse hierarchical designs.
	Library of Parametrized Modules (LPM)	●	●	●						●	●	●		The LPM offers parametrized functions that can be used as building blocks to simplify design entry.
	MegaCore Functions							●					●	MegaCore functions are pre-verified HDL design files for complex, system-level functions that are created by Altera and optimized for Altera device architectures.
Design Compilation	Timing-Driven Synthesis & Fitting		●	●			●	●		●	●	●		Timing-driven synthesis & fitting allows you to specify timing constraints for any portion of the design, thereby controlling MAX+PLUS II synthesis and fitting.
	Logic Synthesis & Fitting	●	●	●						●	●	●		Logic synthesis & fitting ensures optimal device utilization by automatically matching design requirements with device resources, eliminating manual routing.
	Automatic Error Location	●	●	●						●	●	●		The Message Processor quickly locates and highlights syntax and logic errors in all design editors for swift design debugging.
	Design-Rule Checking		●	●	●					●	●	●		The Design Doctor checks designs with customizable design rules and flags potentially unreliable circuitry.
	Multi-Device Partitioning		●	●	●					●	●	●		Multi-device partitioning automatically divides large designs into two or more devices from the same family.
	OpenCore™ Evaluation	●	●	●						●	●	●		OpenCore evaluation enables designers to compile and simulate MegaCore and AMPP functions before licensing the function.
Design Verification	Timing Analysis	●	●	●						●	●	●		The Timing Analyzer traces all possible signal paths to determine the speed-critical and performance-limiting paths of a design.
	Waveform Editing	●	●	●						●	●	●		The Waveform Editor allows designers to create a file containing the input waveforms that drive simulation and the node names to be simulated, and then view the simulation results.
	Functional Simulation	●	●	●						●	●	●		The Simulator uses design information to model the logical function of a design with zero propagation delays.
	Timing Simulation		●	●	●					●	●	●		The Simulator tests the logical function and worst-case timing of a fully synthesized and optimized design to a resolution of 0.1 ns.
	Multi-Device Simulation		●	●	●					●	●	●		The Simulator allows designs partitioned into multiple devices to be simulated together.
Device Programming	Device Programming	●	●	●						●	●	●		Together with the appropriate programming hardware, the MAX+PLUS II software programs, configures, verifies, examines, blank-checks, and functionally tests Altera devices on your desktop. It supports in-system programmability (ISP), in-circuit reconfigurability (ICR), and traditional programming methods.
	Jam™ Programming and Test Language	●	●	●						●	●	●		MAX+PLUS II software supports the Jam programming and test language, which is an interpreted language optimized for programming devices via the IEEE 1149.1 standard JTAG interface.
Other	Floating Node Capability			●						●	●	●		Floating node capability allows multiple users to share a single design site over a network.
	On-Line Help	●	●	●						●	●	●		MAX+PLUS II Help provides complete documentation for MAX+PLUS II features, design guidelines, and detailed device information. It is also available in Japanese.
	ES Site License	●	●	●						●	●	●		The ES Site License entitles you to install an unlimited number of MAX+PLUS II design sites with an entry-level feature set.

* See page 4 for a complete list of MegaCore migration products.

Blue-shaded areas represent design sites (indicated by a PLS prefix). Unshaded areas represent migration products (PLSM prefix).

Step 2 – Add MegaCore Migration Products

As PLDs reach higher density levels, design flows must be as efficient as possible. Altera addresses this need by being the industry leader in providing reusable and synthesizable megafunctions—called MegaCore functions—that are targeted for popular PLD applications.

MegaCore functions are developed, pre-tested, documented and licensed by Altera as MAX+PLUS II migration products. These functions are optimized for specific Altera device architectures, and allow you to rapidly implement the functions you need rather than building them from the ground up.

Altera's MegaCore functions support applications such as PCI and other bus interfaces, digital signal processing (DSP), and communications. The table below lists the functions available today.

Altera expands and updates its MegaCore function offerings regularly. For the latest information on MegaCore functions, go to the Altera world-wide web site at **http://www.altera.com**.

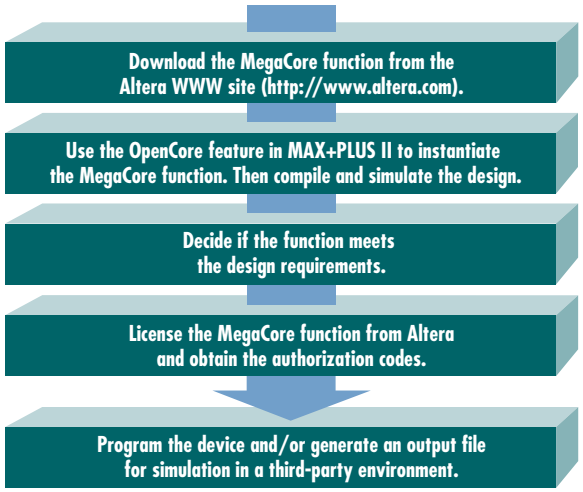
Altera OpenCore Feature

The Altera OpenCore evaluation feature, available with all MAX+PLUS II development tools, offers designers with a no-risk means of evaluating MegaCore and AMPP functions. The OpenCore feature allows you to instantiate, compile, and simulate your designs to verify that a function fits your design needs. Once you evaluate a MegaCore function, you can license it and receive the authorization code, which enables the MAX+PLUS II software to generate programming files, as well as EDIF, VHDL, or Verilog HDL netlist files for simulation in third-party EDA tools.

Download MegaCore Functions at No Cost

Designers can download MegaCore functions for OpenCore evaluation from the Altera world-wide web site at **http://www.altera.com**. The following figure shows the typical MegaCore function design flow:

Design Flow for Using MegaCore Functions



Altera MegaCore Functions

APPLICATIONS	ORDERING CODE	FUNCTION
PCI Master-Target Interface	PLSM-PCI/A	PCI master-target interface with internal DMA engine and zero-wait state burst mode operation at 33 MHz
PCI Target Interface	PLSM-PCIT1	PCI target interface with zero-wait state burst mode operation of unlimited length at 33 MHz
DSP/Fast Fourier Transform	PLSM-FFT	Fully parameterized fast Fourier transform function
Microperipheral Functions	PLSM-MICROLIB	Library of UART, DMA controller, and parallel port controller functions
	PLSM-8237	Programmable DMA controller
	PLSM-8251	Programmable communications interface
	PLSM-8255	Programmable peripheral interface adapter
	PLSM-6402	Universal asynchronous receiver/transmitter
	PLSM-16450	Universal asynchronous receiver/transmitter
	PLSM-6850	Asynchronous communications interface adapter
	PLSM-8259	Programmable interrupt controller
Video/Color Space Converter	PLSM-CSC	RGB-to-YCrCb and YCrCb-to-RGB color space converters
Communications/ Error Checking	PLSM-CRC	Fully parameterized cyclic redundancy code generator and checker

Step 3 – Add Software Maintenance

Altera enhances and improves its development tools regularly. The software maintenance program ensures that you receive the newest version of the MAX+PLUS II development software every quarter, which will help you expand your Altera development system and automatically benefit from Altera's ongoing product developments.

The Altera software maintenance program provides the following benefits:

■ New Device Support

Altera remains at the forefront of PLD development, offering the highest density and highest performance devices in the industry. Altera regularly expands its device and package options, which allows you to design your system with the most advanced devices and packages.

■ New Software Features

Altera's innovation involves all aspects of PLD technology, including design methodology. New software features and enhancements make the MAX+PLUS II software easier to use and improve design compilation times. Users with maintenance agreements receive new features with each MAX+PLUS II update, ranging from HDL synthesis—which is now provided as a standard feature—to improved timing-driven compilation performance.

■ Programming Methodology

Altera is committed to incorporating the latest programming methods, including in-system programmability (ISP), in-circuit reconfigurability (ICR), and the Jam programming and test language. Altera continues to enhance its programming hardware and software to make these programming methods easily accessible.

■ Third-Party EDA Interfaces

The MAX+PLUS II software provides interfaces to all major EDA design tools as a standard feature. These interfaces allow you to work in the design environment you know best and implement your design in the Altera device family you choose. Altera continually enhances the MAX+PLUS II design environment to stay current with third-party EDA tool improvements and upgrades.

Maintenance Ordering Method

Use the following table to select the appropriate maintenance product for your MAX+PLUS II software. Identify your platform and MAX+PLUS II system configuration, and then choose the corresponding maintenance product (e.g., if you own PLS-BASE and one migration product, your maintenance product is PLAESW-BASE).

MAX+PLUS II Maintenance Products

Platform	System Configuration		Maintenance Product
	Design Site	No. of Migration Products*	
PC	PLS-BASE	1	PLAESW-BASE
	PLS-BASE	2 or More	PLAESW-PC
	PLS-MAGNUM	–	PLAESW-PC
	PLS-NET/PC	–	PLAESW-FLOAT
UNIX Workstation	PLS-WS/SN	–	PLAESW-FLOAT
	PLS-WS/HP	–	PLAESW-FLOAT
	PLS-WS/IBMRS	–	PLAESW-FLOAT

* MegaCore function migration products do not count toward the number of migration products used to determine the appropriate maintenance product.

Step 4 – Select the Appropriate Programming Hardware

Altera's ByteBlasterMV™ Parallel Download Cable and BitBlaster™ Serial Download Cable (PL-BYTEBLASTERMV and PL-BITBLASTER) are available for in-circuit reconfiguration of FLEX 10K, FLEX 8000, and FLEX 6000 devices, and in-system programming of MAX 9000 and MAX 7000 devices. These cables download device data from the MAX+PLUS II software or directly from a system prompt.

The Altera Stand-Alone Programmer (PL-ASAP2), used with the appropriate programming adapters, provides the hardware and software needed for programming all Altera devices. PL-ASAP2 includes an LP6 Logic Programmer card for Windows-based PC and compatible computers, a Master Programming Unit (MPU), and programming software.

Use the following table to select the appropriate programming adapters for your devices; adapters for new devices are available when the devices are introduced.

DEVICE(S)	PACKAGE	ADAPTER
EPC1064 *(1)*	DIP, J-Lead	PLMJ1213
EPC1064V *(1)*	TQFP	PLMT1064
EPC1441 *(2)*		
EPC1 *(2)*	DIP	PLMJ1213
EPC1213 *(2)*	J-Lead	PLMJ1213
EPM9320	J-Lead (84-pin)	PLMJ9320-84
	RQFP (208-pin)	PLMR9000-208
	PGA (280-pin)	PLMG9000-280
EPM9320A	J-Lead (84-pin)	PLMJ9320-84
	RQFP (208-pin)	PLMR9000-208NC *(3)*
EPM9400	J-Lead (84-pin)	PLMJ9400-84
	RQFP (208-pin)	PLMR9000-208
	RQFP (240-pin)	PLMR9000-240
EPM9480	RQFP (208-pin)	PLMR9000-208
	RQFP (240-pin)	PLMR9000-240
EPM9560	RQFP (208-pin)	PLMR9000-208
	RQFP (240-pin)	PLMR9000-240
	PGA (280-pin)	PLMG9000-280
	RQFP (304-pin)	PLMR9000-304
EPM9560A	RQFP (208-pin)	PLMR9000-208NC *(3)*
	RQFP (240-pin)	PLMR9000-240NC *(3)*
EPM7032	J-Lead (44-pin)	PLMJ7000-44
EPM7032V	PQFP (44-pin)	PLMQ7000-44
	TQFP (44-pin)	PLMT7000-44
EPM7032S	J-Lead (44-pin)	PLMJ7000-44
EPM7032AE	TQFP (44-pin)	PLMT7000-44
EPM7064	J-Lead (44-pin)	PLMJ7000-44
	TQFP (44-pin)	PLMT7000-44
	J-Lead (68-pin)	PLMJ7000-68
	J-Lead (84-pin)	PLMJ7000-84
	PQFP (100-pin)	PLMQ7000-100
EPM7064S	J-Lead (44-pin)	PLMJ7000-44
EPM7064AE	J-Lead (84-pin)	PLMJ7000-84
	TQFP (44-pin)	PLMT7000-44
	TQFP (100-pin)	PLMT7000-100NC *(3)*
EPM7096	J-Lead (68-pin)	PLMJ7000-68
	J-Lead (84-pin)	PLMJ7000-84
	PQFP (100-pin)	PLMQ7000-100
EPM7128	J-Lead (84-pin)	PLMJ7000-84
EPM7128E	PQFP (100-pin)	PLMQ7000-100
	PQFP (160-pin)	PLMQ7128/7160-160
EPM7128A	J-Lead (84-pin)	PLMJ7000-84
	TQFP (100-pin)	PLMT7000-100NC *(3)*
	TQFP (144-pin)	PLMT7000-144NC *(3)*
EPM7128S	J-Lead (84-pin)	PLMJ7000-84
	PQFP (100-pin)	PLMQ7000-100NC *(3)*
	TQFP (100-pin)	PLMT7000-100NC *(3)*
	PQFP (160-pin)	PLMQ7128/160-160NC *(3)*
EPM7160E	J-Lead (84-pin)	PLMJ7000-84
	PQFP (100-pin)	PLMQ7000-100
	PQFP (160-pin)	PLMQ7128/7160-160
EPM7160S	J-Lead (84-pin)	PLMJ7000-84
	PQFP (100-pin)	PLMQ7000-100NC *(3)*
	PQFP (160-pin)	PLMQ7128/160-160NC *(3)*
EPM7192E	PGA (160-pin)	PLMG7192-160
	PQFP (160-pin)	PLMQ7192/7256-160
EPM7192S	PQFP (160-pin)	PLMQ7192/256-160NC *(3)*
EPM7256E	PQFP (160-pin)	PLMQ7192/7256-160
	PGA (192-pin)	PLMG7256-192
	PQFP (208-pin)	PLMR7256-208
	RQFP (208-pin)	PLMR7256-208
EPM7256A	PQFP (208-pin)	PLMR7256-208NC *(3)*
EPM7256S	RQFP (208-pin)	PLMR7256-208NC *(3)*
EPM7384AE	TQFP (144-pin)	PLMT7000-144NC *(3)*
	PQFP (208-pin)	PLMR7256-208NC *(3)*
EPM7512AE	TQFP (144-pin)	PLMT7000-144NC *(3)*
	PQFP (208-pin)	PLMR7256-208NC *(3)*
EPM5032	DIP	PLMD5032A
	J-Lead	PLMJ5032A
	SOIC	PLMS5032A
EPM5064	J-Lead	PLMJ5064A
EPM5128	J-Lead	PLMJ5128A
	PGA	PLMG5128A
EPM5130	J-Lead	PLMJ5130A
	PGA	PLMG5130A
	PQFP	PLMQ5130A
EPM5192	J-Lead	PLMJ5192A
	PGA	PLMG5192A
EP1810	DIP	PLED1810
	J-Lead	PLEJ1810 *(4)*
EP610	SOIC	PLES610 *(4)*
	DIP	PLED610 *(4)*
	J-Lead	PLEJ610 *(4)*
EP910	J-Lead	PLEJ910 *(4)*
	PGA	PLEG910 *(4)*

(1) FLEX 8000 Configuration EPROM.
(2) FLEX 10K, FLEX 8000, or FLEX 6000 Configuration EPROM.
(3) These devices are not shipped in carriers.
(4) Any device that requires a programming adapter identified with a PLE ordering code prefix also requires a PLAD3-12 compatibility adapter.

ES Site License & PLS-WEB Design Site

Altera offers the ES Site License program, which entitles your company to install an unlimited number of MAX+PLUS II design sites with an entry-level feature set. You will receive the ES Site License once you purchase a PC-based version of the MAX+PLUS II design site.

Altera also offers the PLS-WEB design site, which is an entry-level version of the MAX+PLUS II software. You can download PLS-WEB for free from the Altera world-wide web site at **http://www.altera.com**.

To take advantage of the Altera ES Site License or the PLS-WEB design site, you must first register and obtain a software authorization code from the Altera world-wide web site.

The ES Site License and PLS-WEB design site support MAX 7000 and Classic+Plus devices, as well as the following features:

- Schematic and AHDL design entry
- Library of parameterized modules (LPM)
- OpenCore evaluation
- EDA interfaces
- Floorplan editing
- Hierarchical design management
- Logic synthesis and fitting
- Automatic error location
- Timing analysis
- Device programming
- On-line help

Recommended System Configurations

The following chart shows the recommended standard system configurations for using the Altera development software tools listed in this guide.

Recommended System Configurations

Memory Requirements

Device Family	Minimum Available Memory (Mbytes)	Minimum Physical RAM (Mbytes)
FLEX 10K	256	128
FLEX 6000	64	32
FLEX 8000	64	32
MAX 9000	64	32
MAX 7000	48	16

Windows-Based PC

- Pentium-based PC or compatible computer
- Operating system software:
  - Microsoft Windows NT version 3.51 or higher
    or
  - Microsoft Windows 95 or Windows 98
- SVGA graphics card and monitor compatible with Microsoft Windows
- CD-ROM drive
- 2- or 3-button mouse compatible with Microsoft Windows
- Full-length 8-bit ISA slot for programming card
- Parallel port
- HTML browser (e.g., Netscape Navigator)

Sun SPARCstation

- Sun SPARCstation with color or monochrome monitor
- Sun Solaris version 2.5 or higher
- ISO 9660-compatible CD-ROM drive
- HTML browser (e.g., Netscape Navigator)

HP 9000 Series 700/800 Workstation

- HP 9000 Series 700/800 workstation with color or monochrome monitor
- HP-UX version 10.20 or higher
- HP-CDE
- ISO 9660-compatible CD-ROM drive
- HTML browser (e.g., Netscape Navigator)

IBM RISC System/6000 Workstation

- IBM RISC System/6000 workstation with color or monochrome monitor
- AIX version 4.1 or higher
- ISO 9660-compatible CD-ROM drive
- HTML browser (e.g., Netscape Navigator)

ACCESS Program & Partners

Altera's Commitment to Cooperative Engineering Solutions (ACCESS) program includes EDA vendors who have developed design entry, synthesis, verification, and/or device programming products that support Altera's programmable logic device families. Through this program, Altera supports the industry-standard EDA tools common to many of today's design environments.

Altera is continually evaluating and adding new ACCESS partners to benefit customers.

Interfaces to Synopsys, Cadence, Synplicity, Exemplar, Viewlogic, and Mentor Graphics tools are provided on all MAX+PLUS II CD-ROMs. Contact Altera about interfaces to other ACCESS partner tools.

ACCESS Partners & Supported Tools

CADENCE
- Composer
- Concept
- Leapfrog
- NC-Verilog
- Synergy
- Verilog-XL

EXEMPLAR LOGIC
- Galileo Extreme
- Leonardo Spectrum

MENTOR GRAPHICS
- Design Architect
- FPGA Station
- PLDSynthesis
- QuickSim II
- Quick VHDL
- QuickHDL Pro

SYNOPSYS
- Design Compiler
- DesignWare
- FPGA Compiler
- FPGA Express
- Motive
- SmartModels (Logic Modeling Group)
- VCS
- VHDL Compiler
- VHDL System Simulator (VSS)

SYNPLICITY
- HDL Analyst
- Synplify

VIEWLOGIC
- IntelliFlow
- Motive
- SpeedWave
- Vantage VHDL
- VCS
- WorkView Office

OTHER ACCESS PARTNERS
- Accel Technologies
- ACEO Technology
- Acugen Software
- Aldec
- Flynn Systems
- IKOS Systems
- i-Logix
- ISDATA
- Logical Devices
- Mentor Graphics
- MINC
- Model Technology
- OrCAD
- Simucad
- Sophia Systems and Technology
- Summit Design
- Veda Design Automation
- VeriBest
- Vista Technologies

ACCESS℠ PROGRAM

Altera Megafunction Partners Program

AMPP℠

Altera has developed the Altera Megafunction Partners Program (AMPP) alliance to provide a broad portfolio of Altera-optimized megafunctions that facilitate high-density design. AMPP partners are highly trained on Altera's tools and device architectures to help ensure that their products meet our customers' needs. AMPP megafunctions range from simple building-block logic to very complex system-level cores, such as Reed-Solomon CODECs.

Altera Consultants Alliance Program

ACAP℠

The Altera Consultants Alliance Program (ACAP) is designed to provide expert design assistance to Altera PLD users and help them quickly get their products to market. ACAP consultants are highly trained on Altera devices and tools; Altera carefully selects each ACAP consultant based on their knowledge of Altera devices, tools, and their design background. By recruiting a diverse group of consultants, Altera offers a group of experts who can help designers accelerate their design cycle times.

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M-SG-TOOLS-12

The Altera Advantage