Component Selector Guide

April 1998

The Broadest Range of Programmable Logic Solutions

In today's changing marketplace, time-to-market is the key to success. The company that gets to market first is usually the company that wins. At Altera, we're in business to help companies get to market first. Altera's product offerings address many of today's most critical design needs, such as fast system performance, low cost, and high density. The Altera programmable logic solution is the broadest and most flexible alternative to gate arrays for volume production.

Altera offers a range of programmable logic device (PLD) families to fit your needs, including the FLEX® 10K, FLEX 6000, FLEX 8000, MAX® 9000, and MAX 7000 families. Altera devices are the fastest high-density PLDs available, with in-system speeds of over 100 MHz and pin-to-pin delays as fast as 5 ns. In addition, Altera devices offer advanced system-level features such as embedded array blocks (EABs) and in-system programmability (ISP).

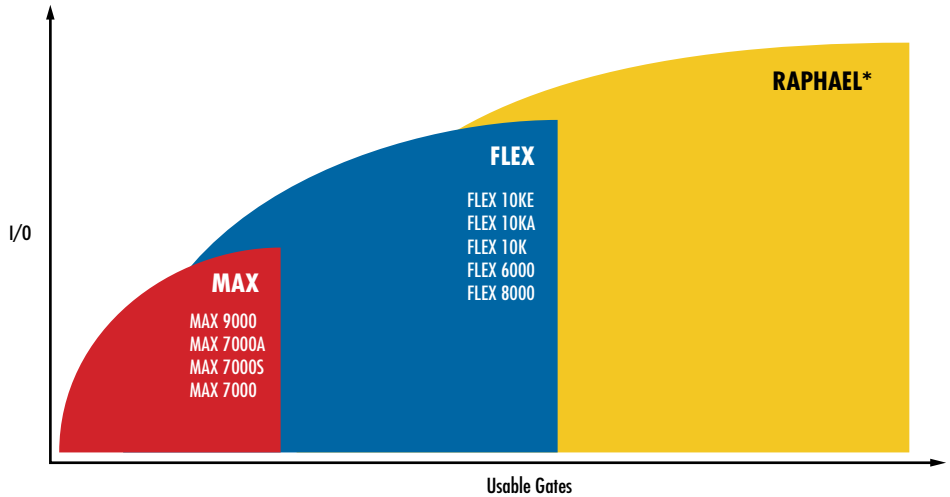
With features such as MultiVolt™ I/O—which allows easy interfacing between 5.0-V, 3.3-V, and 2.5-V hybrid systems—and densities ranging from 600 up to 250,000 gates, Altera devices are designed to support changing design needs. From address decoders to entire systems-on-a-chip, Altera provides a solution for your individual design requirements.

As a technology leader, Altera utilizes the most advanced CMOS processes as they become available and support reliable manufacturing. This process migration enhances performance and reduces manufacturing costs, enabling Altera to offer faster and more cost-effective devices. Additionally, each process advancement allows for lower power dissipation at a given device density.

Altera devices are available in a broad range of space-saving package options, including the innovative FineLine BGA™ and thin quad flat pack (TQFP) packages.

In addition to its high-performance devices, Altera offers powerful development tools to complete your design solution. Altera's MAX+PLUS® II software provides an integrated, easy-to-use development tool that supports all Altera device families. The MAX+PLUS II software is compatible with industry-standard EDA tools and provides direct VHDL, Verilog HDL, and EDIF interfaces.

Product Families



	MAX 7000	MAX 9000	FLEX 8000	FLEX 6000	FLEX 10K	Raphael*
Usable Gates	600-20,000	6,000-12,000	2,500-16,000	10,000-24,000	10,000-250,000	Up to 2,000,000
Performance (MHz)**	178	145	125	125	166	250
Pin Count	44-256	84-356	84-304	100-256	84-672	Up to 1,000

* Preliminary. Contact Altera for latest information.
** Counter frequency (16-bit, up/down loadable counter).

Raphael Family

Altera recently announced Raphael, a revolutionary new PLD architecture with up to two million gates, more than 15 times the capacity of the largest PLDs on the market today. The Raphael architecture extends the benefits of Altera's three-dimensional interconnect structure to a fourth level, further improving speed and die area by leveraging additional process metal layers. This revolutionary MultiCore™ architecture will enable the implementation of complex, high-performance system-on-chip functionality using a single PLD.

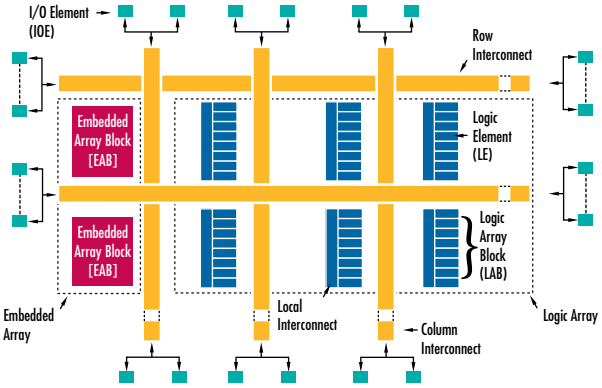
FLEX Families

By combining the time-to-market advantages of PLDs with the density, speed, and cost once associated exclusively with gate arrays, Altera's FLEX devices are the most advanced, high-performance, and cost-effective gate array replacements available today.

FLEX 10K Family

Ranging from 10,000 to 250,000 gates with up to 166-MHz system performance (16-bit counter benchmark), FLEX 10K devices combine the flexibility of programmable logic with the performance and density of embedded gate arrays. With its unique logic implementation structures—the embedded array and logic array—FLEX 10K revolutionizes programmable logic architectures.

FLEX 10K Block Diagram



The FLEX 10K family is the first programmable logic device family with an embedded array.

Each embedded array consists of embedded array blocks (EABs). Each EAB provides up to 4 Kbits of fast-access memory and is therefore ideal for ROMs, FIFOs, and asynchronous, synchronous, and dual-port RAM. The logic array contains logic array blocks (LABs), each of which consists of eight enhanced logic elements (LEs) that communicate through a local interconnect. Each LE contains a four-input look-up table (LUT), a programmable register, and dedicated paths for carry and cascade functions.

Both EABs and LABs interact through the FastTrack Interconnect™, a series of fast, continuous metal lines that run the entire length and width of the device. This metal-friendly architecture efficiently maps to multiple process metal layers, achieving maximum performance with minimum silicon area and cost. Each FastTrack row and column feeds multiple I/O elements (IOEs), which contain an I/O register with flexible control signals, programmable slew rate control, and one output enable per pin.

3.3-V FLEX 10KA devices extend the FLEX 10K architecture up to 250,000 gates using a 0.35-micron, 4-layer-metal, CMOS SRAM process that further increases performance, lowers power consumption, and lowers costs.

FLEX 10K Highlights

FEATURE	BENEFIT
Over 100-MHz system performance	Programmable solution for today's high-speed, high-bandwidth designs
PCI compliance	Meets all specifications of the PCI local bus
Hierarchical FastTrack Interconnect	Fast, predictable interconnect delays
Dual-port RAM (FLEX 10KE devices only)	Individual read/write ports on EABs for simultaneous read/write capability
Density up to 250,000 gates	Addresses 90% of all gate array design starts
Embedded array blocks	Convenient on-chip RAM that allows the user to implement complex megafunctions
2.5-V, 3.3-V & 5.0-V device options	Supports multiple operating voltages
MultiVolt I/O operation	Ideal for mixed-voltage systems
FineLine BGA™ packaging	Area-optimized, high-pin-count BGA offering
Vertical migration	Addresses changing design density needs without the need to re-spin the board

FLEX 10KE devices further enhance the FLEX 10K embedded architecture. Built on a 2.5-V, 0.25-micron, 5-layer-metal process, FLEX 10KE devices offer 66-MHz PCI performance and enhanced dual-port RAM capability. These enhancements provide new levels of performance and efficiency for a variety of on-chip memory requirements and complex megafunctions.

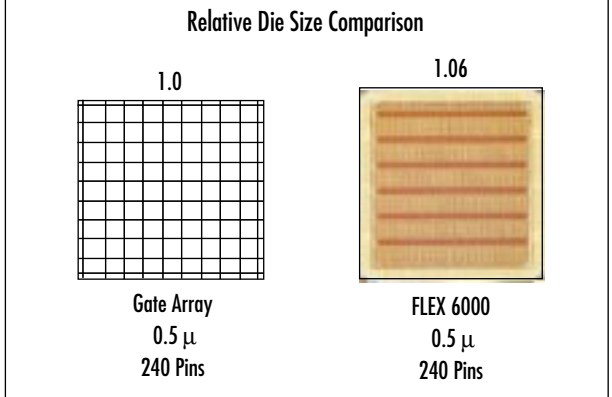
FLEX 6000 Family

The FLEX 6000 family, which offers both 5.0-V and 3.3-V devices, delivers the performance, flexibility and time-to-market of programmable logic at prices that are competitive with gate arrays. FLEX 6000 devices feature the industry's most efficient PLD architecture ever designed—OptiFLEX™—and advanced bond pad pitches as small as 3.0 mil (µPitch™). Every OptiFLEX architectural feature is targeted at producing maximum performance and utilization in the smallest possible die area. This optimization along with µPitch bond pad technology produces a die size that is comparable to that of a gate array and allows for a flexible and cost-effective PLD alternative to ASICs for high-volume production.

FLEX 6000 Highlights

FEATURE	BENEFIT
OptiFLEX architecture	High-performance volume solution that is cost-competitive with gate arrays
PCI compliance	Meets all specifications of the PCI local bus
Interleaved LABs	Leverages speed and flexibility of local interconnects
FastFLEX I/O	Maximizes I/O performance and flexibility
µPitch™ bond pad technology	Minimizes bond pad pitch for maximum die size reduction
3.3-V and 5.0-V device options	Supports multiple operating voltages
MultiVolt I/O operation	Ideal for mixed-voltage systems

FLEX 6000 OptiFLEX Efficiency



The FLEX 6000 logic array contains logic array blocks (LABs) composed of 10 logic elements (LEs) that communicate through a fully populated local interconnect structure. This LAB has been designed to support LAB interleaving, an innovative feature that gives any LE the flexibility to access the local interconnect of its own LAB and adjacent LABs. LAB interleaving leverages the inherent speed and flexibility of local resources, while optimizing global resource usage within the FLEX architecture.

The logic array is routed through Altera's patented FastTrack Interconnect, a series of fast, continuous row and column channels that run the entire length and width of the device. Each row and column feed multiple I/O elements (IOEs), which have a programmable slew-rate and an individual tri-state output enable for each pin. The FLEX 6000 family also supports FastFLEX™ I/O, a feature that provides a direct path from the LE to the I/O pin for fast clock-to-output timing and helps meet the stringent PCI timing requirements.

Today's ASIC designers know that low cost and time-to-market are critical for market success. In the past, designers had to make a tradeoff: use programmable logic for flexibility or use ASICs for low unit cost. The FLEX 6000 family eliminates this tradeoff by providing low-cost flexibility and high performance from initial prototyping through volume production.

FLEX 8000 Family

The FLEX 8000 family offers devices ranging from 2,500 to 16,000 gates and fast, predictable interconnect delays.

The FLEX 8000 architecture consists of silicon-efficient, fine-grained logic elements grouped into high-performance, coarse-grained LABs. This dual granularity enables the FLEX 8000 family to offer both the fast performance of CPLDs and the high resource utilization of gate arrays.

LABs are connected through Altera's FastTrack Interconnect, which is based on continuous row and column interconnect lines. The FastTrack Interconnect eliminates the highly variable, cumulative delays typical of segmented FPGA interconnect structures. With the FLEX 8000 family, you can easily implement applications that require high flipflop counts—such as pipelined data paths and data transformation/compression algorithms—without sacrificing fast system clock rates. PCI-compliant FLEX 8000 devices are ideal for data-intensive applications such as graphics controllers, multimedia cards, networking cards, and communications equipment.

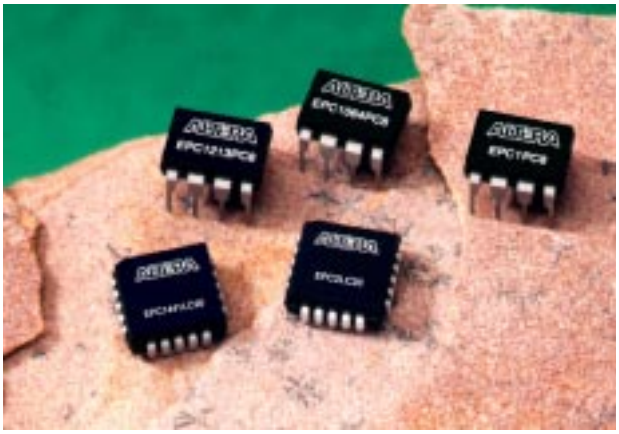
FLEX 8000 Highlights

FEATURE	BENEFIT
FastTrack Interconnect	Fast, predictable interconnect delays
PCI compliance	Meets all specifications of the PCI local bus
MultiVolt I/O operation	Ideal for mixed-voltage systems
JTAG compliance	Enables in-depth board- and system-level testing

Configuration EPROMs

Altera's serial Configuration EPROMs store configuration data for SRAM-based FLEX devices. With devices ranging in density from the 64 Kbit EPC1064 to the reprogrammable 2 Mbit EPC2, the industry's largest Configuration EPROM, Altera provides the widest range of serial configuration devices in the industry.

All FLEX devices can control the entire configuration process and retrieve data from the Configuration EPROMs without the need for an external intelligent controller. Many members of the Configuration EPROM family have the capability to operate at either 3.3 V or 5.0 V. This capability can be controlled by the user through a programmable bit.



Configuration EPROM Highlights

FEATURE	BENEFIT
High density	A 2-Mbit, single-device configuration solution for the highest-density FLEX devices
Low cost	Lowest cost-per-bit solution available in the industry
3.3-V and 5.0-V device options	Supports multiple operating voltages

MAX Device Families

Altera's MAX device families offer solutions for high-speed applications at competitive prices. The high-performance, high-density MAX devices are based on the advanced Multiple Array MatriX (MAX) architecture and offer densities from 600 to 20,000 usable gates. These devices provide solutions for a broad array of high-performance applications, including simple PLD integration.

MAX 7000 Highlights

FEATURE	BENEFIT
5-ns propagation delays	Support fast, high-speed state machines and control logic
PCI compliance	Satisfies PCI bus requirements
600 to 20,000 usable gates	Multiple density options for simple PLD integration
3.3-V and 5.0-V device options	Different device options support both operating voltages
In-system programmability (ISP)	Allows for easy prototyping and in-field upgrades, and simplifies manufacturing flow
Supports Jam programming and test language	Vendor independence, faster programming, and reduced file size
Built-in JTAG support	Simplifies device and system testing
Programmable power-saving mode	Enables >50% power reduction
MultiVolt I/O operation	Ideal for mixed-voltage systems

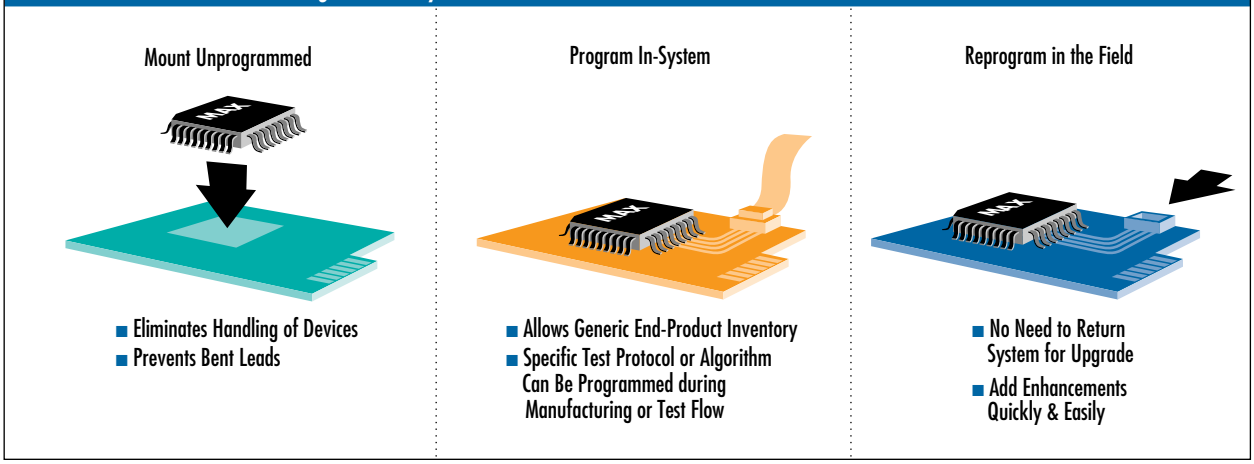
MAX 7000 Family

The MAX 7000 family is the fastest programmable logic solution available in the industry. The CMOS EEPROM-based MAX 7000 devices offer propagation delays as fast as 5 ns, producing counter frequencies in excess of 178 MHz. With PCI-compliant, high-performance devices across the entire product line, MAX 7000 devices are ideal for a variety of high-speed applications.

The MAX 7000 family offers a wide selection of high-density devices, ranging from 32 to 1,024 macrocells. MAX 7000 devices are well-suited for mixed-voltage environments, offering 3.3-V core supply operation with MultiVolt I/O operation that interfaces between 2.5-V, 3.3-V, and 5.0-V devices.

MAX 7000A and MAX 7000S devices offer in-system programmability and support the vendor-independent Jam programming and test language. MAX 7000A devices provide 3.3-V ISP in a broad range of densities, while MAX 7000S devices provide a 5.0-V ISP solution. ISP enables designers to program a device after it is mounted on a printed circuit board. ISP benefits a manufacturing environment by reducing the risk of lead damage and benefits a design environment by allowing designers to make enhancements to a system after it has been manufactured. The Jam programming and test language is useful in both embedded processor and automated

ISP Increases Manufacturing Efficiency



MAX 7000A, MAX 7000S, and MAX 9000 devices provide an industry-standard four-pin JTAG ISP interface for programming a device after it has been mounted on a printed circuit board.

test equipment (ATE) applications, allowing ISP-capable devices to be programmed with smaller file sizes and in less time. MAX 7000A and MAX 7000S devices also have built-in JTAG boundary-scan test circuitry.

Features common to all MAX 7000 devices include global clocking, fast input registers, and programmable slew-rate control. These features allow MAX 7000 devices to address a broad range of system-level applications. High-speed global clocks coupled with 5 ns propagation delays and fast setup times create superior system performance with high-speed, device-to-device communication. The programmable slew-rate control allows system noise to be reduced by slowing the switching time of outputs that are not speed critical. A programmable power-saving feature allows for 50% or greater power reduction in each macrocell.

MAX 9000 Highlights

FEATURE	BENEFIT
10-ns propagation delays	Increases in-system performance to 145 MHz
PCI compliance	Meets all the specifications of the PCI local bus
6,000 to 12,000 usable gates	Improves system integration
In-system programmability (ISP)	Allows for easy prototyping and in-field upgrades, and simplifies manufacturing flow
Pin-to-pin compatibility	Allows migration to different densities without re-layout of board
MultiVolt I/O operation	Ideal for mixed-voltage systems
Supports Jam programming and test language	Ease of use for embedded processor and ATE programming applications

MAX 9000 Family

The MAX 9000 family, which offers densities from 320 to 560 macrocells, is the fastest, 5.0-V PLD family in its density class. MAX 9000 devices are ideal for high-speed applications, offering pin-to-pin delays as fast as 10 ns with typical in-system performance of 145 MHz (16-bit, up/down loadable counter). In addition, MAX 9000 devices offer PCI compliance.

The MAX 9000 family builds on the success of Altera's popular MAX 7000 family, while offering up to 560 macrocells and maintaining the industry's leading performance.

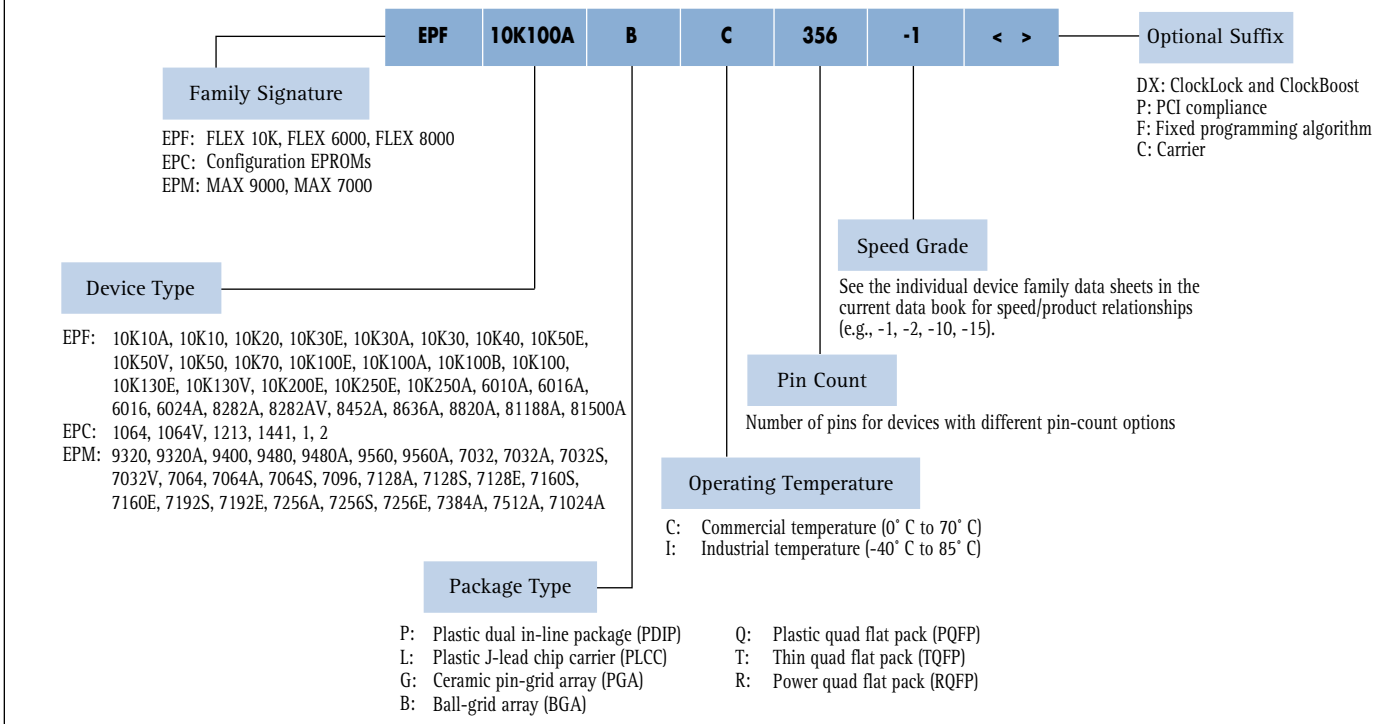
In addition to high-performance and density, MAX 9000 devices offer the latest features to address the most complex design challenges, including PCI compliance, in-system programmability (ISP), support for built-in Joint Test Action Group (JTAG) boundary-scan test, and MultiVolt I/O.

Ordering Altera Devices

The following tables list the devices available for each Altera family as well as the Configuration EPROMs for FLEX devices. The diagram below provides an explanation of Altera part numbers.

Use this diagram together with the device tables to select the appropriate device, pin/package options, supply voltage, and speed grade.

Product Ordering Information



FLEX 10K Devices

DEVICE[1]	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	LOGIC ELEMENTS	RAM BITS
EPF10K10	10,000	84-Pin PLCC, 144-Pin TQFP, 208-Pin PQFP	59, 102, 134	5.0 V	-3, -4	576	6,144
EPF10K10A	10,000	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	66[2], 102, 134, 150[2]	3.3 V	-1, -2, -3	576	6,144
EPF10K20	20,000	144-Pin TQFP, 208-Pin RQFP, 240-Pin PQFP	102, 147, 189	5.0 V	-3, -4	1,152	12,288
EPF10K30	30,000	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	147, 189, 246	5.0 V	-3, -4	1,728	12,288
EPF10K30A	30,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-pin BGA[1], 356-Pin BGA, 484-Pin BGA[1]	102, 147, 189, 191[2], 246, 246[2]	3.3 V	-1, -2, -3	1,728	12,288
EPF10K30E	30,000	144-Pin TQFP, 208-Pin PQFP, 256-pin BGA[1], 484-pin BGA[1]	102, 147, 176[2], 220[2]	2.5 V	-1, -2, -3	1,728	24,576
EPF10K40	40,000	208-Pin RQFP, 240-Pin RQFP	147, 189	5.0 V	-3, -4	2,304	16,384
EPF10K50	50,000	240-Pin RQFP, 356-Pin BGA, 403-Pin PGA	189, 274, 310	5.0 V	-3, -4	2,880	20,480
EPF10K50V	50,000	240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[1]	189, 274, 310[2]	3.3 V	-1, -2, -3, -4	2,880	20,480
EPF10K50E	50,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[1], 484-Pin BGA[1]	102, 147, 189, 191[2], 256[2]	2.5 V	-1, -2, -3	2,880	40,960
EPF10K70	70,000	240-Pin RQFP, 503-Pin PGA	189, 358	5.0 V	-2, -3, -4	3,744	18,432
EPF10K100	100,000	503-Pin PGA	406	5.0 V	-3, -4	4,992	24,576
EPF10K100A	100,000	240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[1], 600-pin BGA	189, 274, 371[2], 406	3.3 V	-1, -2, -3	4,992	24,576
EPF10K100B	100,000	208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[1]	147, 189, 191[2]	2.5 V	-1, -2, -3	4,992	24,576
EPF10K100E	100,000	208-Pin PQFP, 240-Pin PQFP, 256-pin BGA[1], 484-pin BGA[1]	147, 189, 191[2], 340[2]	2.5 V	-1, -2, -3	4,992	49,152
EPF10K130V	130,000	599-Pin PGA, 600-Pin BGA	470, 470	3.3 V	-2, -3, -4	6,656	32,768
EPF10K130E	130,000	240-Pin PQFP, 484-Pin BGA[1], 672-Pin BGA[1]	186, 371[2], 426[2]	2.5 V	-1, -2, -3	6,656	65,536
EPF10K200E	200,000	240-Pin RQFP, 599-Pin PGA, 672-pin BGA[1]	182, 470, 470[2]	2.5 V	-1, -2, -3	9,984	98,304
EPF10K250A	250,000	599-Pin PGA, 600-Pin BGA	470, 470	3.3 V	-1, -2, -3	12,160	40,960
EPF10K250E	250,000	240-Pin RQFP, 599-Pin PGA, 672-Pin BGA[1]	179, 470, 470[2]	2.5 V	-1, -2, -3	12,160	81,920

Notes: [1] Space-saving FineLine BGA™ package.
[2] Preliminary. Contact Altera for latest information.

FLEX 6000 Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	FLIP-FLOPS	LOGIC ELEMENTS
EPF6010A	10,000	100-Pin TQFP, 144-Pin TQFP	81, 117	3.3 V	-1, -2, -3	880	880
EPF6016	16,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA	117, 171, 199, 204	5.0 V	-2, -3	1,320	1,320
EPF6016A	16,000	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	81, 117, 171, 218[2]	3.3 V	-1, -2, -3	1,320	1,320
EPF6024A	24,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA, 256-Pin BGA[1]	117, 171, 199, 218, 218[2]	3.3 V	-1, -2, -3	1,960	1,960

Notes: [1] Space-saving FineLine BGA™ package.
[2] Preliminary. Contact Altera for latest information.

FLEX 8000 Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	FLIP-FLOPS	LOGIC ELEMENTS
EPF8282A	2,500	84-Pin PLCC, 100-Pin TQFP	68, 78	5.0 V	-2, -3, -4	282	208
EPF8282AV	2,500	100-Pin TQFP	78	3.3 V	-3, -4	282	208
EPF8452A	4,000	160-Pin PQFP	120	5.0 V	-2	452	336
EPF8452A	4,000	84-Pin PLCC, 100-Pin TQFP, 160-Pin PGA/PQFP	68, 120	5.0 V	-3, -4	452	336
EPF8636A	6,000	208-Pin PQFP	136	5.0 V	-2	636	504
EPF8636A	6,000	84-Pin PLCC, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP	68, 118, 136	5.0 V	-3, -4	636	504
EPF8820A	8,000	144-Pin TQFP, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP	112, 120, 152	5.0 V	-2	820	672
EPF8820A	8,000	144-Pin TQFP, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP, 225-Pin BGA	112, 120, 152	5.0 V	-3, -4	820	672
EPF81188A	12,000	208-Pin PQFP, 232-Pin PGA, 240-Pin PQFP	148, 184	5.0 V	-2, -3, -4	1,188	1,008
EPF81500A	16,000	240-Pin PQFP, 280-Pin PGA, 304-Pin RQFP	181, 208	5.0 V	-2, -3, -4	1,500	1,296

Configuration EPROMs for FLEX Devices

DEVICE	PIN/PACKAGE OPTIONS	SUPPLY VOLTAGE	DESCRIPTION
EPC1064	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	5.0 V	64-Kbit serial EPROM designed to configure FLEX 8000 devices.
EPC1064V	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	3.3 V	64-Kbit serial EPROM designed to configure FLEX 8000 devices.
EPC1213	8-Pin PDIP, 20-Pin PLCC	5.0 V	213-Kbit serial EPROM designed to configure FLEX 8000 devices.
EPC1441[1]	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	3.3/5.0 V	441-Kbit serial EPROM designed to configure all FLEX devices.
EPC1[1]	8-Pin PDIP, 20-Pin PLCC	3.3/5.0 V	1-Mbit serial EPROM designed to configure all FLEX devices.
EPC2[1]	20-Pin PLCC, 32-Pin TQFP	3.3/5.0 V	2-Mbit serial EPROM designed to configure all FLEX devices.

Note: [1] This device can be programmed by the user to operate at either 3.3 V or 5.0 V.

MAX 7000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM7032A	32	44-Pin PLCC/TQFP	36	3.3 V	-5, -7, -10
EPM7032S	32	44-Pin PLCC/TQFP	36	5.0 V	-6, -7, -10
EPM7032	32	44-Pin PLCC/TQFP/PQFP	36	5.0 V	-6, -7, -10, -12, -15
EPM7032V	32	44-Pin PLCC/TQFP	36	3.3 V	-12, -15, -20
EPM7064A	64	44-Pin PLCC/TQFP, 100-Pin TQFP, 100-Pin BGA[1]	38, 68, 68	3.3 V	-5, -7, -10
EPM7064S	64	44-Pin PLCC/TQFP, 84-Pin PLCC, 100-Pin PQFP/TQFP	36, 52, 68	5.0 V	-5, -6, -7, -10
EPM7064	64	44-Pin PLCC/TQFP, 68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	36, 52, 68	5.0 V	-6, -7, -10, -12, -15
EPM7096	96	68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	52, 64, 76	5.0 V	-7, -10, -12, -15
EPM7128A	128	84-Pin PLCC, 100-Pin TQFP, 100-Pin BGA[1], 144-Pin TQFP, 256-Pin BGA[1]	68, 84, 84, 100, 100	3.3 V	-5, -6, -7, -10
EPM7128S	128	84-Pin PLCC, 100-Pin PQFP/TQFP, 160-Pin PQFP	68, 84, 100	5.0 V	-6, -7, -10, -15
EPM7128E	128	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	5.0 V	-7, -10, -12, -15, -20
EPM7160S	160	84-Pin PLCC, 100-Pin TQFP, 160-Pin PQFP	64, 84, 104	5.0 V	-7, -10, -15
EPM7160E	160	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 104	5.0 V	-10, -12, -15, -20
EPM7192S	192	160-Pin PQFP	124	5.0 V	-7, -10, -15
EPM7192E	192	160-Pin PQFP/PGA	124	5.0 V	-12, -15, -20
EPM7256A	256	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	84, 120, 164, 164	3.3 V	-6, -7, -10
EPM7256S	256	208-Pin RQFP/PQFP	132, 164	5.0 V	-7, -10, -15
EPM7256E	256	160-Pin PQFP, 192-Pin PGA, 208-Pin RQFP	132, 164	5.0 V	-12, -15, -20
EPM7384A	384	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	120, 176, 212	3.3 V	-7, -10, -15
EPM7512A	512	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	120, 176, 212	3.3 V	-7, -10, -15
EPM71024A	1,024	208-Pin PQFP, 256-Pin BGA[1]	176, 212	3.3 V	-7, -10, -15

Note: [1] Space-saving FineLine BGA™ package.

MAX 9000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM9320A	320	84-Pin PLCC, 208-Pin RQFP, 356-Pin BGA	60, 132, 168	5.0 V	-10, -15
EPM9320	320	84-Pin PLCC, 208-Pin RQFP, 280-Pin PGA, 356-Pin BGA	60, 132, 168	5.0 V	-15, -20
EPM9400	400	84-Pin PLCC, 208-Pin RQFP, 240-Pin RQFP	59, 139, 159	5.0 V	-15, -20
EPM9480A	480	208-Pin RQFP, 240-Pin RQFP	146, 175	5.0 V	-10, -15
EPM9480	480	208-Pin RQFP, 240-Pin RQFP	146, 175	5.0 V	-15, -20
EPM9560A	560	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	153, 191, 216	5.0 V	-10, -15
EPM9560	560	208-Pin RQFP, 240-Pin RQFP, 280-Pin PGA, 304-Pin RQFP, 356-Pin BGA	153, 191, 216	5.0 V	-15, -20

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