

I²C Interface Megafunctions

Solution Brief 31

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Target Applications:

Bus & Interfaces

Processor & Peripherals

Family:

FLEX[®] 10K & FLEX 6000

Vendor:



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Features

- Two megafunctions available
 - I²C Master Interface megafunction
 - I²C Slave Interface megafunction
- Byte write operating mode
- Random access read operating mode
- Spike filter
- Writeable 32-bit data register
- Writeable 16-bit configuration register
- Readable 16-bit data register

General Description

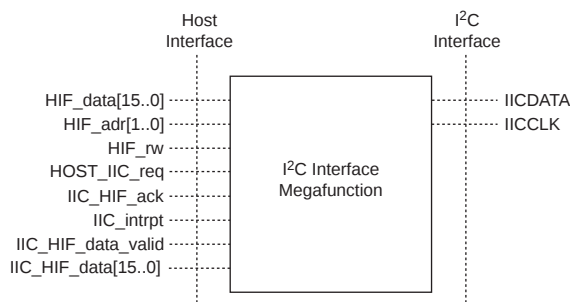
The Inter Integrated Circuit (I²C) Master Interface and I²C Slave Interface megafunctions are general-purpose interfaces used to connect several peripheral devices to one controlling unit. They can support active devices with different clock domains. A key advantage of these megafunctions is that a device other than a CPU can be defined as the master on the I²C bus. These megafunctions are ideal for automotive applications.

Functional Description

The I²C Interface megafunctions interface a parallel bus to a standard I²C serial bus. The I²C Master Interface megafunction connects a host CPU to the I²C bus, and the I²C Slave Interface megafunction connects a peripheral data bus to a serial I²C bus. Both megafunctions manage timing as well as data framing and error handling.

The I²C bus allows a host CPU to configure external devices using a proprietary bus and removes obstacles such as different clock domains. To implement an I²C bus, you must connect an I²C Master Interface megafunction to the host CPU and an I²C Slave Interface megafunction to each external device located on the bus. Figure 1 shows a block diagram of the I²C Interface megafunctions.

Figure 1. I²C Interface Megafunctions Block Diagram



The I²C Master Interface megafunction includes three registers for communication between the host CPU and the I²C bus:

- Writeable 32-bit data register
- Writeable 16-bit configuration register
- Readable 16-bit data register

Writeable 32-Bit Data Register

The 32-bit writeable data register consists of two 16-bit registers, `data_reg_high[31..16]` and `data_reg_low[15..0]`, that handle the 16-bit data bus of the host CPU. At the beginning of a read / write access, the CPU loads the 32-bit data register with the data required to transfer data on the I²C bus. This information consists of a 7-bit device code, an 8-bit address, 8 bits of data, and read / write bits. The remaining bits are unused. The data transfer on the I²C bus always begins when `data_reg_low[15..0]` has been loaded.

Writeable 16-Bit Configuration Register

The 16-bit writeable configuration register contains configuration information, such as interrupt masking, that can be changed by the host CPU. This register includes the reference frequency for the clock signal generation for the I²C bus. The I²C Interface megafunction supports 90-kHz frequency in the standard mode.

Readable 16-Bit Data Register

The 16-bit readable data register contains the 8-bit data received from the I²C bus in random access read mode. This register also contains an error bit, an interrupt bit, and a write-allowed bit. The error bit signals a failed data transfer, and the interrupt bit signals that the register has new data that must be read by the host CPU. The interrupt bit is generated without respect to the `irq` bit in the configuration register.

The IICCLK signal can be stalled by any I²C device to prevent data from being transmitted via the I²C bus. If the IICCLK signal is stalled during a write access, the next write access will not be acknowledged. To prevent this event, the 16-bit readable data register provides a write-allowed bit, which is set to 0 to indicate that the writeable 32-bit data register is ready for a new write access.

Ports

Tables 1, 2, and 3 describe both megafunctions' global signals, interface signals to the host CPU, and interface signals to the I²C bus, respectively.

Table 1. I²C Interface Megafunctions Global Signals

Name	Type	Description
<code>clk_27</code>	Input	27-MHz clock signal.
<code>Reset_n</code>	Input	Active-low synchronized reset signal.

Table 2. Interface Signals to the Host CPU

Name	Type	Description
<code>HIF_data[15..0]</code>	Input	16-bit data bus from the host CPU.
<code>HIF_adr[1..0]</code>	Input	2-bit address bus.
<code>HIF_rw</code>	Input	Read/write select. A 0 indicates a write, and a 1 indicates a read.
<code>HOST_IIC_req</code>	Input	Host CPU requests for the next read/write access
<code>IIC_HIF_ack</code>	Output	Acknowledge. The I ² C Interface megafunction is ready for a new request.
<code>IIC_intrpt</code>	Output	Interrupt. Data must be read from the data register of the I ² C Interface megafunction.
<code>IIC_HIF_data_valid</code>	Output	Data valid on the bus.
<code>IIC_HIF_data[15..0]</code>	Output	16-bit data bus to the host CPU.

Table 3. Interface Signals to the I²C Bus

Name	Type	Description
IICDATA	Input/Output	Data for the I ² C Interface megafunction.
IICCLK	Input/Output	Clock for the I ² C Interface megafunction.

Utilization

Tables 4 and 5 describe both megafunctions' logic cell requirements for FLEX 10K and FLEX 6000 devices.

Table 4. I²C Master Interface Megafunction Logic Cell Requirements

Device Family	Smallest Device	Speed Grade	Logic Cells	EABs (1)	f _{MAX} (MHz)	Availability
FLEX 10K	EPF10K20	-3, -4	243	0	39	Now
FLEX 6000	EPF6016	-2	308	—	29	Now

Table 5. I²C Slave Interface Megafunction Logic Cell Requirements

Device Family	Smallest Device	Speed Grade	Logic Cells	EABs (1)	f _{MAX} (MHz)	Availability
FLEX 10K	EPF10K20	-3, -4	122	0	38	Now
FLEX 6000	EPF6016	-2	135	—	32	Now

Note to tables:

(1) EAB = embedded array block

Deliverables

The I²C Interface package includes the following for each megafunction:

- MAX+PLUS® II Text Design File (.tdf) netlist
- MAX+PLUS II Parameterized Symbol File (.sym)
- Engineering documentation
 - Interface description
 - Sample application
 - Configuration register
 - Timing diagrams

For more information on the I²C Interface package, contact SICAN Microelectronics directly.



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