

CAN Bus Megafunction

Solution Brief 22

September 1997, ver. 1

Target Applications:

Bus & Interfaces
Processor & Peripherals

Family:

FLEX® 10K & FLEX 8000

Vendor:



Sican Microelectronics Corp.
400 Oyster Point Blvd. Suite 512
S. San Francisco, CA 94080
Tel. (415) 871-1494
FAX (415) 871-1504
WWW <http://www.SICAN-micro.com>

Features

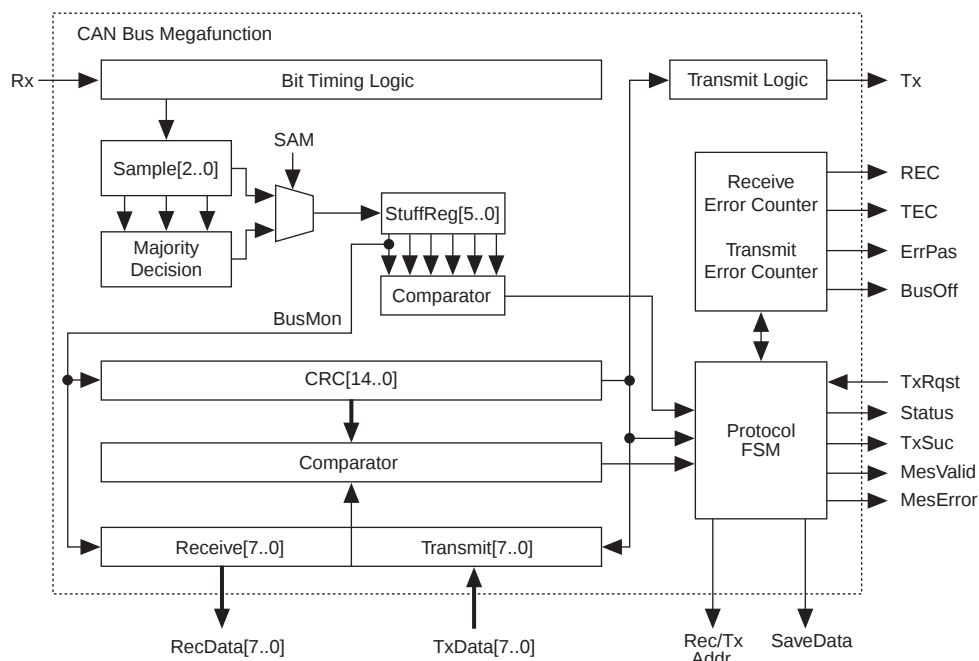
- Compatible with Controller Area Network (CAN) Specification 2.0A and 2.0B passive / active
- Completely synchronous flipflop design
- Individual acceptance filtering
- Self-test mode
- Readable error counters
- Data transfer rate up to 1 Mbit / second
- Cycle frequency of 12 MHz

General Description

The CAN bus megafunction fulfills all protocol functions according to CAN Specification 2.0B, including extended functionality (CAN Specification 2.0B active). The megafunction offers three acceptance filtering options: basic CAN protocol (the mask and code register is similar to the Philips 82C200 CAN controller), full CAN protocol (similar to the Intel 82527 CAN controller), and a combination of the basic and full protocols. The CAN bus megafunction incorporates all the features required by CAN Specification 2.0, including error handling capabilities, stuff bit generation, cyclic redundancy code (CRC), and multiple sample points.

The CAN bus megafunction has a universal interface for connecting to the receive and transmit buffers, allowing the megafunction to be optimized for specific applications. This megafunction is ideal for a variety of applications, including automotive electronics, home automation, or simple sensor / actuator systems. Figure 1 shows a block diagram of the CAN bus megafunction.

Figure 1. CAN Bus Megafunction Block Diagram



Functional Description

The base module performs the task of a CAN controller according to CAN Specification 2.0B. The base module has no receive buffer memory.

CAN Bus Interface

A simple two-wire connection is the interface to the CAN bus, i.e., the RX input pin and the TX output pin. Both connections operate at the TTL level and are appropriate for operation with CAN bus transceivers according to ISO / DIS 11898 (e.g., Phillips PCA 82C250, Bosch CF150, or Siliconix SI 9200), or with a modified RS-485 interface.

Error Counter

The CAN protocol contains a mechanism for automatic fault location to switch off defective nodes. This mechanism consists of two error counters for the receive and transmit modes: the receive error counter (REC) and the transmit error counter (TEC). These counters are incremented or decremented according to CAN Specification 2.0.

Error Protection

Each telegram contains a 15-bit-wide CRC code that is generated from the actual data in the preceding telegram sections (i.e., the start of frame, arbitration field, control field, and data field sections). Upon receipt, the actual data is compared with the code contained in the telegram. If the CRC code and actual data do not match, the megafunction sends an error telegram.

Bitstream Processor/Internal Interface

Data can be sent in parallel to the base module via an 8-bit-wide data bus. The base module converts the data blocks into a serial bitstream. When the base module encounters five bits in a row with the same polarity, it inserts a stuff bit with opposite polarity into the bitstream, forcing the necessary edges for resynchronization. The stuff register filters stuff bits from the received bitstream. Then, the bitstream is transmitted to the interface module.

Acceptance Filtering

The megafunction offers three acceptance filtering options: acceptance filtering with one or more identifiers indicated explicitly (full CAN), acceptance filtering with a mask register (basic CAN), or a combination of both full and basic CAN.

Interrupts

The megafunction can implement one or more interrupt outputs that are triggered when one of the following events occur:

- Megafunction becomes error passive
- Megafunction reaches the status “Bus Off”
- Error counters exceed a programmable level
- Telegram is sent successfully
- Telegram is received successfully
- Receive memory overflows

Utilization

Table 1 describes the logic cell requirements for FLEX 10K and FLEX 8000 architectures.

Table 1. CAN Bus Megafunction Logic Cell Requirements						
Device Family	Smallest Device	Speed Grade	Logic Cells	EABs	f _{MAX}	Availability
FLEX 10K	EPF10K20	-3	720	0	12 MHz	Now
FLEX 8000	EPF8820A	-2	720	Note (1)	12 MHz	Now

Note:

(1) FLEX 8000 devices do not have embedded array blocks (EABs).

For more information on the CAN bus megafunction, contact Sican Microelectronics directly.



101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
<http://www.altera.com>

Copyright © 1997 Altera Corporation. Altera, FLEX, FLEX 10K, FLEX 8000, EPF10K20, EPF8820A, and AMPP are trademarks and /or service marks of Altera Corporation in the United States and other countries. Other brands or products are trademarks of their respective holders. The specifications contained herein are subject to change without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services. All rights reserved.