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## Application Notes

AN 84 Implementing fft with On-Chip RAM in FLEX 10K Devices

AN 86 Implementing the pci\_a Master/Target in FLEX 10K Devices

AN 101 Improving Performance in FLEX 10K Devices with the Synplify Software

## Brochures

MegaCore Functions Brochure

Quartus Brochure

## Catalogs

LPM Quick Reference Guide

## Data Sheets

a16450 Universal Asynchronous Receiver/Transmitter Data Sheet

a6402 Universal Asynchronous Receiver/Transmitter Data Sheet

a6850 Asynchronous Communications Interface Adapter Data Sheet

a8237 Programmable DMA Controller Data Sheet

a8251 Programmable Communications Interface Data Sheet

a8255 Programmable Peripheral Interface Adapter Data Sheet

a8259 Programmable Interrupt Controller Data Sheet

Altera Programming Hardware Data Sheet

BitBlaster Serial Download Cable Data Sheet

ByteBlaster Parallel Port Download Cable Data Sheet

ByteBlasterMV Parallel Port Download Cable Data Sheet

crc MegaCore Function Parameterized CRC Generator/Checker Data Sheet

fft Fast Fourier Transform Data Sheet

FLEX 10K PCI Prototype Board Data Sheet

MAX+PLUS II Programmable Logic Development System & Software Data Sheet

PCI Master/Target MegaCore Function with DMA Data Sheet

pci\_b PCI Master/Target MegaCore Function Data Sheet  
pcit1 PCI Target MegaCore Function Data Sheet  
RGB2YCrCb & YCrCb2RGB Color Space Converters Data Sheet

## General Information

EDA Software Support  
In-Circuit Test Vendor Support  
Introduction (to the *1998 Data Book*)  
Introduction to Megafunctions  
Ordering Information

## Manuals

MAX+PLUS II Getting Started Manual

## Solution Briefs

SB 12 Fast Fourier Transform MegaCore Function  
SB 20 PCI Bus Master/Target MegaCore Function  
SB 21 a8259 Programmable Interrupt Controller MegaCore Function  
SB 23 Microperipheral MegaCore Library  
SB 27 RGB2YCrCb & YCrCb2RGB Color Space Converter MegaCore Functions  
SB 30 crc MegaCore Function Parameterized CRC Generator/Checker

## Selector Guides

Development Tools Selector Guide  
Megafunctions Selector Guide

## Technical Briefs

TB 25 Using the OpenCore Evaluation Feature  
TB 30 Authorization Codes Now Via the WWW  
TB 35 Download the PLS-WEB MAX+PLUS II Software for Free  
TB 36 Timing-Driven Compilation Improvements in MAX+PLUS II Version 8.2  
TB 39 Using Synopsys Design Compiler & FPGA Compiler to Synthesize Designs for MAX+PLUS II Software  
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- TB 43 Using the MAX+PLUS II Software with Exemplar Logic Leonardo Software
- TB 44 Using Synplicity Synplify Software to Synthesize Designs for MAX+PLUS II Software
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- TB 49 Generating Post-Route Files in the MAX+PLUS II Software for Third-Party Verification

## **User Guides**

PCI MegaCore Function User Guide