

December 1998

## Application Notes

- AN 41 PCI Bus Applications in Altera Devices
- AN 42 Metastability in Altera Devices
- AN 51 Using Programmable Logic for Gate Array Designs
- AN 71 Guidelines for Handling J-Lead & QFP Devices
- AN 73 Implementing FIR Filters in FLEX Devices
- AN 74 Evaluating Power for Altera Devices
- AN 81 Reflow Soldering Guidelines for Surface-Mount Devices
- AN 87 Configuring FLEX 6000 Devices
- AN 92 Understanding FLEX 6000 Timing

## Brochures

- Corporate Brochure
- FLEX 6000 Brochure
- Packaging Solutions Brochure

## Data Sheets

- Altera Device Package Information Data Sheet
- Altera Programming Hardware Data Sheet
- BitBlaster Serial Download Cable Data Sheet
- ByteBlaster Parallel Port Download Cable Data Sheet
- ByteBlasterMV Parallel Port Download Cable Data Sheet
- Configuration EPROMs for FLEX Devices Data Sheet
- Configuration Elements Data Sheet
- FLEX 6000 Programmable Logic Device Family Data Sheet
- Operating Requirements for Altera Devices Data Sheet

## General Information

Introduction (to the Altera *1998 Data Book*)

Ordering Information

## Catalogs

AMPP Catalog

LPM Quick Reference Guide

## Product Information Bulletins

PIB 23 Digital Signal Processing in FLEX Devices

## Selector Guides

Component Selector Guide

## Solution Briefs

SB 21 a8259 Programmable Interrupt Controller MegaCore Function

SB 23 Microperipheral MegaCore Library

SB 30 crc MegaCore Function Parameterized CRC Generator/Checker

SB 31 I<sup>2</sup>C Interface Megafunctions

SB 33 Viterbi Decoder Megafunction

SB 37 64-Bit PCI Bus Target Megafunction

## Technical Briefs

TB 3 FLEX Devices as Alternatives to ASSPs & ASICs

TB 4 Using FLEX Devices as DSP Coprocessors

TB 8 Implementing Multirate Filters in FLEX Devices

TB 9 Advantages of Hybrid I/O for Mixed-Voltage Systems

TB 24 The Advantages of LPM

TB 27 Evaluating FLEX 6000 Performance