Quartus

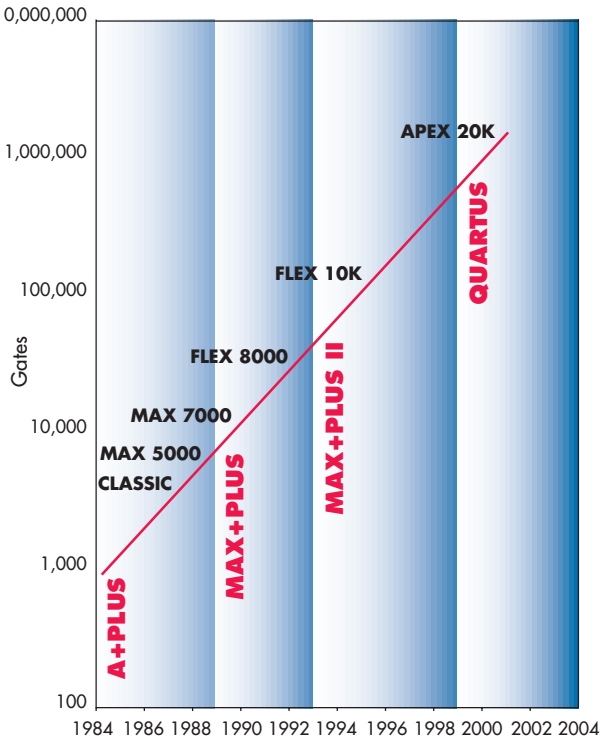
The Next-Generation Development System for Programmable Logic

October 1998

Design Tools for Increasing Device Densities

As device densities increase, design methodologies for programmable logic devices (PLDs) must continue to evolve. The Quartus™ software, Altera's fourth-generation development system for programmable logic, allows designers to process multi-million gate designs with advancements never before seen in PLD development tools. With the Quartus software, Altera continues its commitment to provide development software with unmatched flexibility and performance.

Figure 1. Quartus Software Supports High-Density Design Methodology



The Quartus software offers new process advances that use state-of-the-art features—such as multi-processor support and incremental recompiling—to shorten design cycles. To streamline the development flow and increase productivity, the Quartus software supports system-on-a-chip methodology with block-level editing, workgroup computing, and expanded support for megafunctions. A new logic analysis solution reduces verification time by enabling engineers to see internal chip signal values while the system is running at speed. Quartus software also interfaces seamlessly with third-party EDA software tools, allowing designers to use the tools they are already familiar with to design for Altera® devices. As the industry's first "Internet-aware" development tool, the Quartus software provides up-to-the-minute information and file exchanges, including software updates, license file delivery, and support services across the Internet. Altera effectively becomes a member of the design team by providing an unmatched level of technical support. Together, these features make Quartus software the ideal platform for multi-million gate designs.

Shortened Compilation Times with the nSTEP Compiler

Complex designs often require several design iterations to achieve desired results. Before Quartus software, designers needed to perform a full compilation with each iteration before they could examine results. Now, the Quartus nSTEP™ Compiler allows designers to make changes and obtain results without running a full compilation. The Quartus software only compiles the portions of the design that have changed. This powerful feature significantly shortens compile times and maintains placement and timing in portions of the design that are unchanged.

CoreSyn Synthesis

The nSTEP Compiler uses Altera's new CoreSyn™ synthesis capability. The Compiler analyzes the design and then partitions functions into the appropriate type of look-up table (LUT)-based logic element, product-term-based macrocell, or embedded memory logic block within the APEX™ architecture. Using the CoreSyn capability, the nSTEP Compiler then invokes the appropriate synthesis technology to optimize the logic for that architecture.

Utilizing the Full Computing Power

With the power of PCs and workstations increasing at incredible rates, design tools must be equipped to take advantage of these benefits. The Quartus software was designed from the ground up to fully utilize these improvements by distributing computer-intensive functions to multiple processors. The Quartus software uses the processing power of multiple processors—locally or across a network—and even across multiple operating systems. This feature saves considerable time during the compilation process.

Collaborative Work Environment

As designs get larger, several engineers may work on a single project. The Quartus software uses a centralized object-oriented database that can be accessed by multiple engineers across a network. Commercially available revision control systems or user-integrated systems within the Quartus software preserve the integrity of design revisions as multiple engineers make changes to the design. This feature allows engineers to work on the same project from different sites without interrupting the design cycle.

Megafunctions for High-Density Design

Creating designs for system-on-a-chip architectures requires efficiency throughout the design cycle. Designers can use functions that have already been tested and optimized to further reduce their design time. Altera users have two primary choices of functions: Altera-created megafunctions—called MegaCore™ functions—that are optimized for Altera device architectures, and megafunctions from the Altera Megafunction Partners Program (AMPP℠). AMPP provides a broad portfolio of Altera-optimized megafunctions that are developed by third-party vendors.

Quartus software will expand the support for megafunctions by enabling instance-specific assignments and greater control over synthesis. Customers can maintain assignments for each instance of a MegaCore or AMPP megafunction in a design rather than for each function.

Risk-Free Evaluation with OpenCore

The Quartus OpenCore™ evaluation feature offers you a risk-free method of evaluating AMPP and MegaCore functions. With the OpenCore feature, you can instantiate, compile, and simulate your designs to verify a function's size and performance before making a licensing decision. MegaCore functions can be downloaded for OpenCore evaluation from the Altera world-wide web site at http://www.altera.com.

Improved Verification Flow and SignalTap Logic Analysis

Design verification has become the longest process in developing multi-million gate designs. The Quartus software reduces verification time by providing tight integration to register transfer level (RTL)-based simulation. The Quartus Simulator can accept TCL, C, and hardware description language (HDL) test-benches.

The Quartus software also easily integrates with third-party simulators, allowing you to choose the most efficient verification flow to fit your needs. In addition to running software simulations, designers can use Altera's SignalTap™ logic analysis to perform hardware debugging.

For many designs, system-level verification is very time-consuming, and sometimes extremely difficult on devices with high I/O ball-grid array packages. SignalTap logic analysis facilitates the verification process by integrating the functionality of a logic analyzer within the software.

Designers can capture internal signals of a device and route them to pins for monitoring using SignalTap logic analysis. The Quartus software inserts a logic analyzer megafunction that incorporates the functionality of a logic analyzer and the triggering options into the design. Data is stored in the device's embedded RAM block and reported to the Quartus waveform viewer via a download cable. The SignalTap logic analysis tool allows the design team to perform this analysis on a device running at actual speed.

SignalTap logic analysis accelerates the verification flow by building upon the fact that programmable logic offers the benefit of shortening design cycles. For verification purposes, PLDs offer specific advantages:

True System-Level Verification

Because PLDs remove the risks associated with silicon changes, multiple verification iterations can be made on PLDs. These iterations can be performed in-system at system clock speeds. Millions of true system vectors can be applied per second to test numerous operating conditions. Also, a PLD implementation enables development to begin earlier on real hardware, rather than on software models or emulators.

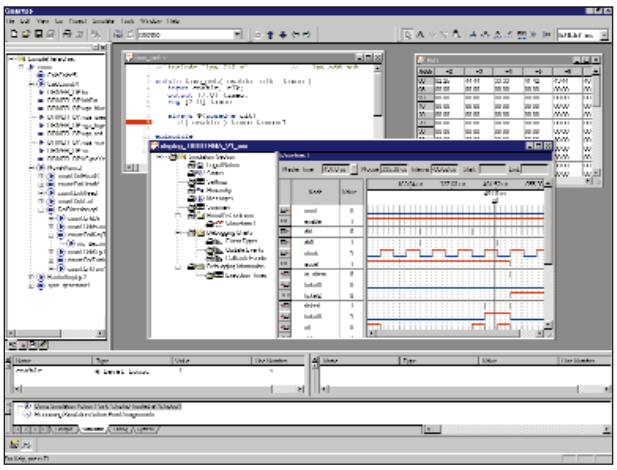
Elimination of the Probing Bottleneck

For PLDs with embedded RAM, a logic analyzer can be implemented in silicon, eliminating the need for an external analyzer. Because it is on-chip, the logic analyzer has full access to any signal in the design. Data is stored in the embedded RAM, and scanned out serially to preserve I/O pins. This data is then assembled on a PC and presented in a waveform display.

Flexibility of PLDs

Changes in the design and in the configuration of the logic analyzer can be made quickly and painlessly with PLDs.

Figure 2. Quartus Verification Interface



Designers can continue using their verification tools and flows with the Quartus software, and avoid the steep learning curve that is typically involved with using a new software tool. They can also take advantage of the innovative SignalTap logic analysis solution to perform system-level verification on chips running at speed. Designs can go into production much faster with these enhancements to the verification process.

NativeLink Integration with Major Design Tools

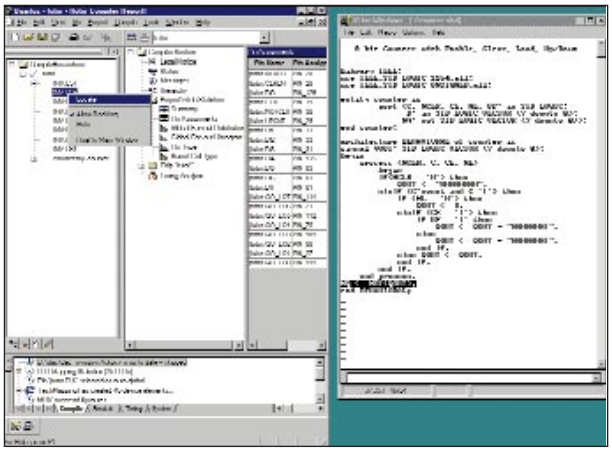
Digital system design flows typically require the use of several different EDA tools to perform tasks from design entry and synthesis to verification and programming. These tools require efficient transfer of information. NativeLink™ integration facilitates the seamless transfer of information between the Quartus software and other EDA tools to enhance the overall productivity of the designer's EDA tool suite.

Altera has worked very closely with major EDA vendors to develop the best interface any PLD software has to offer. Altera opened the Quartus interface to various EDA partners to enable them to provide unmatched levels of integration. NativeLink integration provides a truly seamless interface to major EDA software tools to support existing design flows, eliminating the need to learn new design tools.

Improved Quality of Results

Quartus software provides improved quality of results as well as a variety of features not available in any other tool today. The NativeLink flow allows designers to use Quartus pre-place and route estimates in third-party EDA tools to optimize synthesis strategies. Incremental design changes do not require a total recompilation of the design, further streamlining the design process.

Figure 3. NativeLink Example



Error-Location Capability

While most interfaces allow design information to be passed from one tool to another, they provide little or no interaction between tools. Using the Quartus software, error location and correction is easier than ever before. The Quartus software can identify the source of errors in the EDA tool's source design file, and the errors can be corrected directly in the EDA tool.

Internet-Based Support

The Quartus software is engineered with the latest Internet browser. Designers with Internet access can use Quartus software to connect directly to Altera's web site—including the Atlas℠ Solutions database—from within the software. This direct access provides users with immediate solutions, hints, and workarounds to issues they may face during the design cycle.

Customers can also submit service requests directly to Altera Applications and monitor their progress via the internet while in the Quartus software. The design files and user configuration details can automatically be prepared for transfer to Altera. This feature ensures that the Altera Applications engineer working on the issue can accurately duplicate the design environment. With this feature, Altera effectively becomes an active member of the design team.

Automatic notifications of software patches, new device support, and online help updates are communicated on a daily basis by the Quartus software. Users are prompted to download the latest software upgrades. Designers can choose to have the Quartus software update their design site to ensure access to the latest information.

APEX 20K: A Revolutionary Embedded Architecture

APEX™ 20K, Altera's new high-performance, high-density, embedded PLD family that is designed for system-level integration, integrates look-up-table logic, product-term logic, and memory in a single device with densities up to 2 million gates. This revolutionary architecture, called the MultiCore™ architecture, is fabricated on an advanced 0.25-micron SRAM process, and combines and enhances the strengths of the FLEX® 10K, FLEX 6000, and MAX® 7000 architectures to provide an efficient, high-performance solution for system-level applications.

APEX 20K devices are made up of MegaLAB™ blocks which contain 16 logic array blocks (LABs), an advanced embedded structure called an embedded system block (ESB), and a local interconnect that connects all 16 LABs and the ESB without requiring global routing resources. The ESB can be configured as product-term logic, LUT logic, RAM, ROM or content addressable memory (CAM). APEX 20K devices also offer enhanced ClockLock™ and ClockBoost™ circuitry, and support multiple I/O interfacing standards, including LVTTL, LVCMOS, LVDS, GTL/GTL+, and SSTL-3.

The Convenience of Subscription

Customers can purchase development tool subscriptions from Altera for 12-month periods. This annual subscription entitles the customer to the initial installation of the software, as well as all Altera development system updates and releases over the subsequent 12-month period. Customers will receive the latest versions of the Quartus and MAX+PLUS® II software, providing support for all Altera PLDs, new software features, performance enhancements, and the most current online and printed documentation.

With a subscription, designers will gain access to the most cost-effective, fastest, and highest density PLDs in the industry. As new device families, packages, and speed grades become available, customers will automatically receive support for these newest Altera devices.

For more information, please contact your local Altera sales office.

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