

ALTERA®



MAX+PLUS II

Programmable Logic Development Software

December 1997



Unmatched Flexibility and Performance

Long recognized as the best development system in the programmable logic industry, the MAX+PLUS[®] II development software continues to offer unmatched flexibility and performance. The MAX+PLUS II software offers a completely integrated development flow and an intuitive, Windows-based graphical user interface, making it easy to learn and use. With MAX+PLUS II, you can quickly implement and test changes in your design, program Altera programmable logic devices (PLDs) at your desktop, and eliminate the long lead times typically associated with gate arrays.

Seamless Development Flow

The MAX+PLUS II software offers a seamless development flow, allowing you to enter, compile, and simulate your design and program the device using a single, integrated tool, regardless of the Altera device you choose. Simply give a command to initiate this flow.

Design Entry The MAX+PLUS II software supports multiple design entry methods to fit your needs, including schematic capture, text-based design entry using the Altera Hardware Description Language (AHDL), VHDL, Verilog HDL, and waveform design entry. Different types of design files can be integrated into a single design hierarchy that is

ready for synthesis, allowing you to use the best design entry method for each design task.

Click the Start Button, and MAX+PLUS II Will do the Rest.

Synthesis The MAX+PLUS II software eliminates manual design tasks from your design cycle. The software optimizes the use of logic resources, discards redundant logic, and checks your design for system-level errors before compiling the final design. Errors can be automatically located in the source design files. The software automatically fits the design, removing the need for manual place-and-route, and partitions it into multiple devices as needed.

Verification The MAX+PLUS II software offers design verification—including design simulation and timing analysis—for testing the logical operation and internal timing of a design. You have the flexibility and control to perform functional or timing simulation for single- or multiple-device projects. The software can calculate a matrix of point-to-point device delays, determine setup and hold time requirements at device pins, and calculate maximum clock frequency.

Programming Once your design is verified, you are ready to program or configure an Altera device using the programming hardware that interfaces directly with the MAX+PLUS II software. You can complete your project using a single design environment right on your desktop.



MAX+PLUS II Fits Into Your EDA World

If you already have an EDA environment that you are familiar with or would like to verify your PLD design using a tool from another software supplier, the MAX+PLUS II software will support your needs.

As a standard feature, the MAX+PLUS II software interfaces with all major EDA design tools, including tools for gate array designers. You can work in the design environment you know best and implement your design in the Altera device family you choose.

EDA Tool Support Included in MAX+PLUS II

VENDOR	SCHEMATIC DESIGN ENTRY	SYNTHESIS	GATE-LEVEL SIMULATION	BEHAVIORAL SIMULATION	TIMING ANALYSIS
Synopsys	–	FPGA Express Design Compiler FPGA Compiler	–	VSS	–
Cadence	Composer Concept	–	Verilog-XL	LeapFrog Verilog-XL	VeriTime
Mentor Graphics	Design Architect	–	QuickSim II	ModelSim/ QuickHDL	–
Viewlogic	ViewDraw	–	ViewSim	Speedwave VCS	Motive
Synplicity	–	Synplify	–	–	–
Exemplar	–	Galileo Extreme Leonardo	–	–	–

Once the design is captured and simulated using the tool of your choice, you can transfer your file directly into the MAX+PLUS II software for fitting into your target Altera PLD. The MAX+PLUS II software supports industry-standard VHDL and Verilog HDL design descriptions, as well as EDIF netlists generated by your schematic and synthesis tools. You can easily map functions in your EDA environment to functions compatible with the MAX+PLUS II software, and take advantage of the integrated, easy-to-use, MAX+PLUS II graphical interface to fit your design.

After synthesis and fitting, you can transfer your file directly back into your tool of choice for simulation. The MAX+PLUS II system outputs the full-timing VHDL, Verilog HDL, SDF, and EDIF netlists that can be used for post-route device- and system-level simulation.

Megafunctions for High-Density Design

Creating designs for 250,000 gates requires you to be as efficient as possible throughout your design flow. Instead of building your sub-system from the ground up, you can use ready-made, pre-tested, and optimized functional blocks—called megafunctions—to implement specific functions. Megafunctions are pre-verified HDL design files for complex, system-level functions.

Altera Megafunction Partners Program



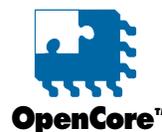
The Altera Megafunction Partners Program (AMPPSM), provides a broad portfolio of Altera-optimized megafunctions, developed by third-party vendors, that facilitate high-density design. All AMPP partners are highly trained on Altera's tools and device architectures to ensure that their products meet our customers' needs. AMPP megafunctions range from functional building-blocks to very complex system-level functions, such as Reed-Solomon CODECs.

MegaCore Functions for Key PLD Applications



Altera provides its own megafunctions—called MegaCoreTM functions—that are optimized for Altera device architectures. MegaCore functions are developed, pre-tested, documented, and licensed by Altera as MAX+PLUS II migration products. Once you license a MegaCore function, you can use it in an unlimited number of design projects without any expiration. Altera MegaCore products offer the functions you need today and focus on key PLD applications—including PCI, DSP, video, and communications.

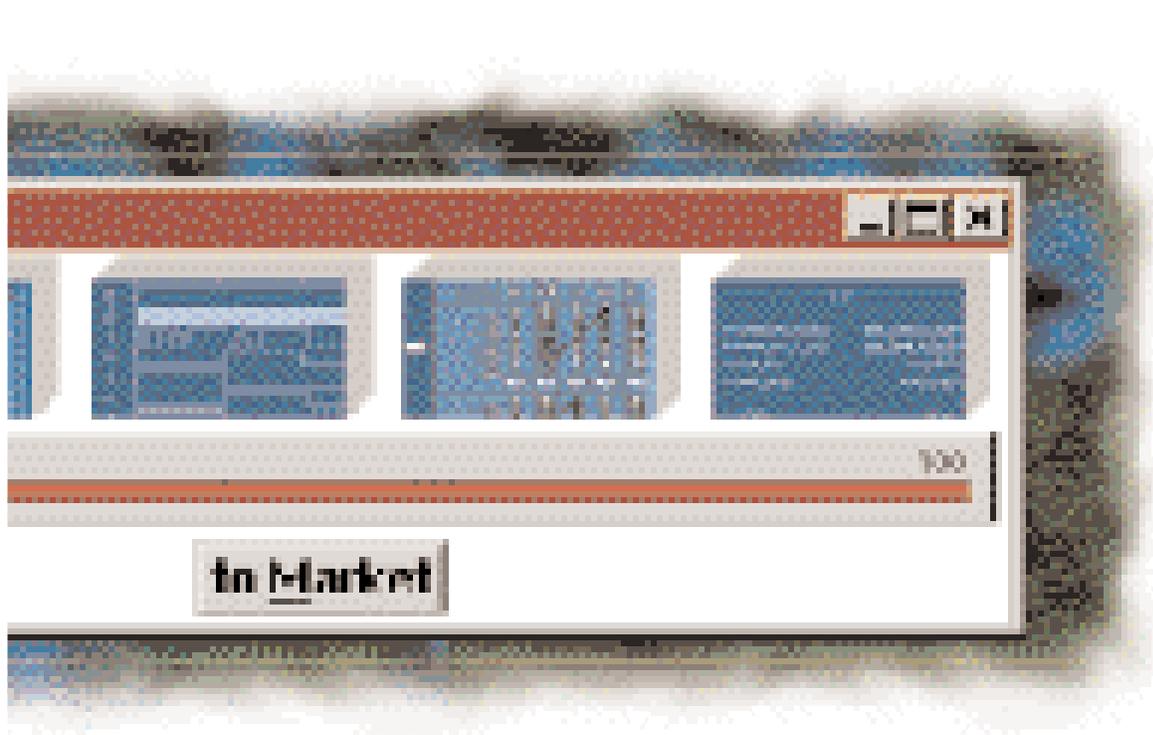
OpenCore Feature for Risk-Free Evaluation



The MAX+PLUS II OpenCoreTM evaluation feature offers you a risk-free method of evaluating AMPP and MegaCore functions. With the OpenCore feature, you can instantiate, compile, and simulate your designs to verify a function's size and performance. You can download MegaCore functions for OpenCore evaluation from the Altera world-wide web site at <http://www.altera.com>.

MegaCore Function Design Flow Using OpenCore Evaluation

1. Download MegaCore function from the Altera web site (www.altera.com).
2. Instantiate the function, then compile and simulate the design.
3. Decide whether the function meets your design requirements.
4. License the function from Altera and obtain the authorization code.
5. Create programming files and optionally generate output files for simulation with third-party EDA tools.



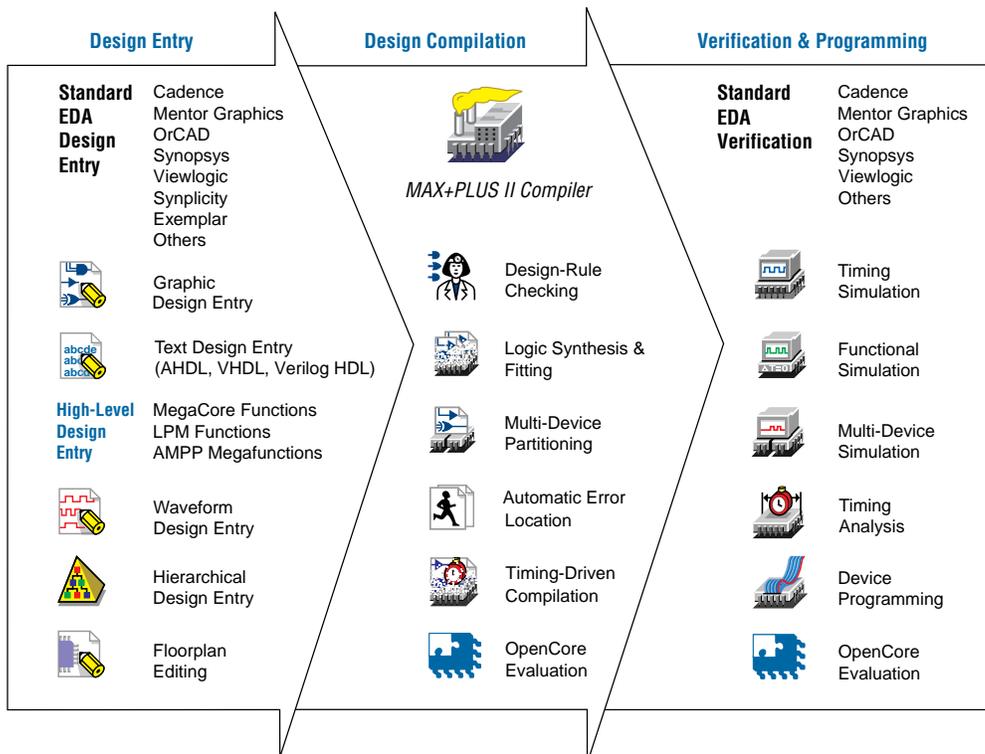
MAX+PLUS II Accelerates Your Design Cycle

The MAX+PLUS II development system compiles your designs dramatically faster than other PLD development tools, allowing you to quickly implement changes and test the results in order to meet your specifications. Because the design cycle is accelerated, you can quickly go through many design iterations.

An average high-density design of up to 100,000 gates can compile in less than 30 minutes, giving you more time to perfect your project.

Get to Market Fast

The MAX+PLUS II integrated design flow, ease-of-use, and fast compilation all work to accelerate your product development process right on your desktop, helping get your product to market in record time.



MAX+PLUS II Design Environment

The MAX+PLUS II design environment offers unmatched flexibility and performance. The software allows for seamless integration with industry-standard design entry, synthesis, and verification tools.

The Maintenance Advantage

Altera enhances and adds features to MAX+PLUS II tools every quarter to increase customers' design productivity. By purchasing maintenance, you will receive quarterly updates to the MAX+PLUS II software with support for the latest Altera PLDs, new software features, performance enhancements, and the most current on-line and printed documentation.

As a maintained user, you will gain access to the least expensive, fastest, and highest density PLDs in the industry. As new device families, packages, and speed grades become available, you will automatically receive support for these newest Altera devices.

Altera ensures that the MAX+PLUS II design environment fosters the best performance and device utilization for Altera PLDs through improvements in compilation speed and quality of results. Maintained users also receive new features in each MAX+PLUS II update, ranging from free HDL synthesis to improved interfaces with third-party EDA tools.

Updated MAX+PLUS II versions also offer the latest programming methodologies, such as in-system programmability (ISP) and support for the Jam™ device programming and test language.

PLS-WEB: Free Development Software

Experience today the many advantages of the MAX+PLUS II software by downloading a free copy of PLS-WEB, an entry-level version of the MAX+PLUS II software tool, from Altera's world-wide web site at <http://www.altera.com>.



Get the Latest Information

For the most up-to-date literature and information on Altera and MAX+PLUS II software, go to the Altera world-wide web site at <http://www.altera.com>.

Altera Offices

Altera Corporation
101 Innovation Drive
San Jose, CA 95134
Telephone: (408) 544-7000
<http://www.altera.com>

Altera European Headquarters
Holmers Farm Way
High Wycombe
Buckinghamshire
HP12 4XF
United Kingdom
Telephone: (44) 1 494 602 000

Altera Japan Ltd.
Shinjuku Mitsui Bldg. 36F
1-1, Nishi-Shinjuku, 2 Chrome
Shinjuku-ku, Tokyo 163-04
Japan
Telephone: (81) 3 3340 9480

Altera International Ltd.
Suites 908-920, Tower 1
MetroPlaza
223 Hing Fong Road
Kwai Fong, New Territories
Hong Kong
Telephone: (852) 2487 2030