

ALTERA®

High Volume

Low Cost

FLEX 6000

High-Volume Solutions for the Gate Array Designer

July 1998

Programmability at Gate Array Prices

Altera's FLEX[®] 6000 programmable logic device (PLD) family delivers the flexibility and time-to-market of programmable logic at prices that are competitive with gate arrays. Featuring the OptiFLEX[™] architecture, the industry's most efficient architecture, FLEX 6000 devices provide a flexible, high-performance, and cost-effective alternative to ASICs for high-volume production.

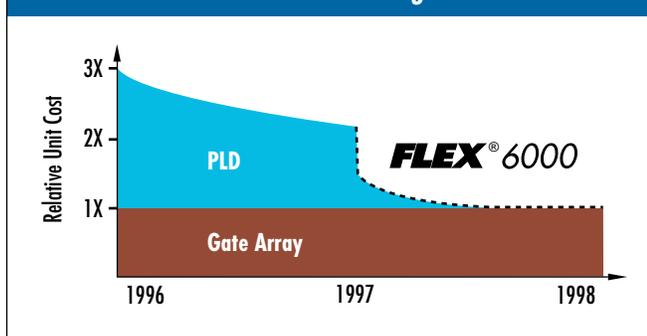
FLEX 6000 Devices

FEATURE	EPF6010A	EPF6016	EPF6016A	EPF6024A
Process Geometry	0.35 μ	0.5 μ	0.35 μ	0.35 μ
Supply Voltage	3.3 V	5.0 V	3.3 V	3.3 V
Pin Migration	Yes	Yes	Yes	Yes
Gate Count	5,000 - 10,000	8,000 - 16,000	8,000 - 16,000	12,000 - 24,000
Logic Elements	880	1,320	1,320	1,960
User I/O Pins (max.)	139	204	171	218
Package Options	100-pin TQFP 100-pin BGA* 144-pin TQFP 256-pin BGA*	144-pin TQFP 208-pin PQFP 240-pin PQFP 256-pin BGA	100-pin TQFP 100-pin BGA* 144-pin TQFP 208-pin PQFP 256-pin BGA*	144-pin TQFP 208-pin PQFP 240-pin PQFP 256-pin BGA 256-pin BGA*

* FineLine BGA[™] package

Today's ASIC designers realize that low cost and time-to-market are critical for market success. In the past, designers were forced to make a tradeoff: use programmable logic for flexibility or use ASICs for low unit cost. But the FLEX 6000 family eliminates this tradeoff by providing low-cost, high-performance flexibility from initial prototyping through volume production.

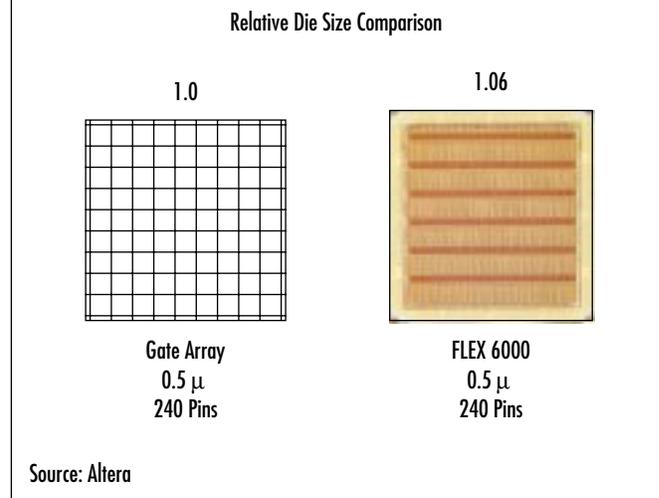
FLEX 6000 Redefines PLD Pricing



OptiFLEX Redefines Programmable Logic Efficiency

Built on either a 3.3-V, 0.35-μ or 5.0-V, 0.5-μ, triple-layer-metal CMOS process, the SRAM-based FLEX 6000 family features the efficient OptiFLEX programmable logic architecture. Every feature in the OptiFLEX architecture is targeted at producing maximum performance and utilization in the smallest possible die area.

FLEX 6000 OptiFLEX Efficiency



The FLEX 6000 logic array contains logic array blocks (LABs) composed of 10 logic elements (LEs) that communicate through a fully populated local interconnect structure. This LAB has been designed to support LAB interleaving, an innovative feature that gives any LE the flexibility to access the local interconnect of its own LAB as well as adjacent LABs. LAB interleaving leverages the inherent speed and flexibility of local resources while optimizing global row and column resource utilization within the FLEX architecture.

Each LE contains a four-input look-up table (LUT), a programmable register, and dedicated paths for carry and cascade functions. The logic array is routed through Altera's patented FastTrack Interconnect[™], a series of fast, continuous row and column channels that run the entire length and width of the device. Each FastTrack row and column feeds multiple I/O elements (IOEs), which have a programmable slew-rate and an individual tri-state output enable control for each pin. The FLEX 6000 family also supports FastFLEX[™] I/O, a feature that provides a direct path from the LE to the I/O pin for fast clock-to-output timing and helps meet stringent PCI timing requirements.

Maximum Die Size Reduction with μPitch Bond Pad Technology

To support costs competitive with gate arrays, Altera combined the OptiFLEX architecture with an advanced 75-μ bond pad pitch. This combination of architecture optimization and μPitch[™] bond pad technology maximizes silicon efficiency, producing a FLEX 6000 die size that is competitive with that of gate arrays.

Low Cost without Sacrificing Performance

Due to the limitations of a segmented architecture, FPGAs must sacrifice both performance and utilization for cost. However, FLEX 6000 devices do not have this constraint. The OptiFLEX architecture optimizes both logic and routing resources while maintaining high performance and utilization. The key is Altera's patented FastTrack Interconnect. By combining interleaved LABs and FastFLEX I/O with a predictable, continuous interconnect structure, FLEX 6000 devices offer higher performance than FPGAs at a significantly lower price.

Flexible Pin Migration

Each FLEX 6000 device is footprint-compatible with other devices in the same package, thus maximizing productivity by supporting concurrent HDL design and board layout. Designs that grow beyond the capacity of a device can easily be migrated to a larger device without requiring a board re-spin. This feature also enables the designer to use a larger device for easy prototyping while maintaining the flexibility to optimize the production design to fit smaller, less-expensive, pin-compatible devices.

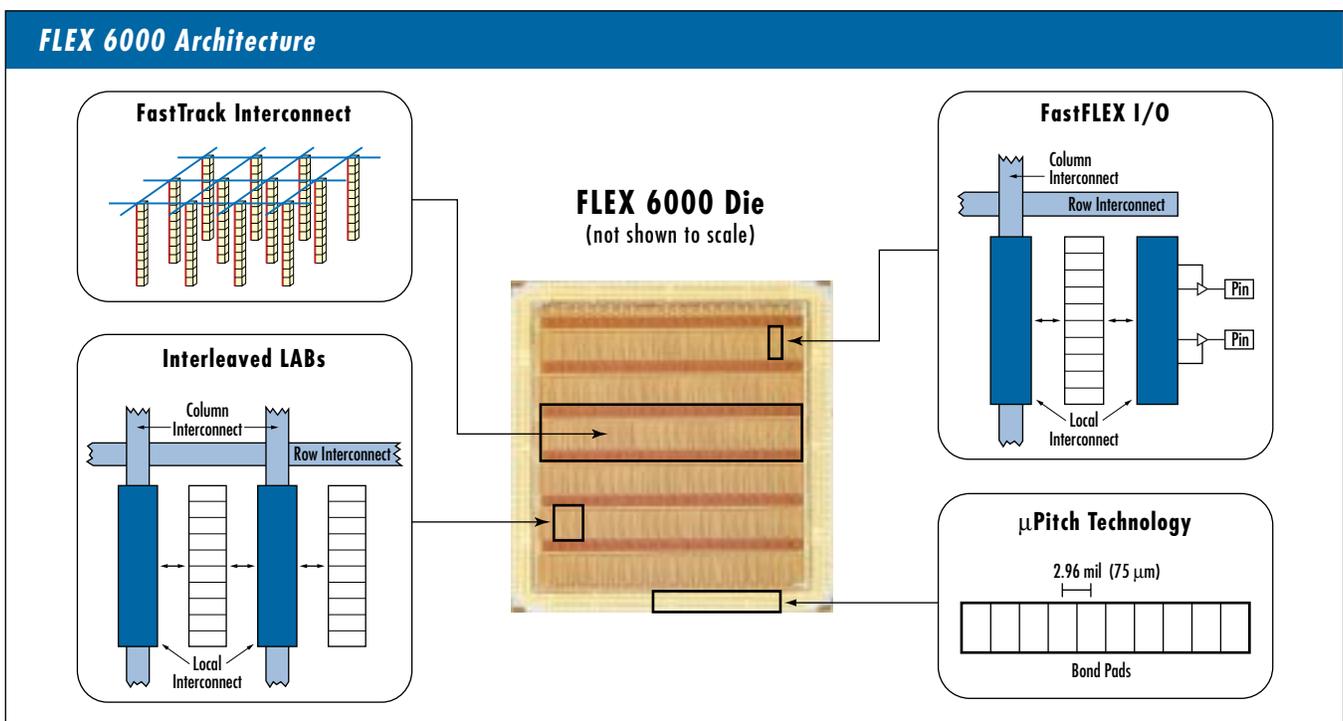
System-Level Features

The FLEX 6000 family contains a number of powerful system-level features that boost design efficiency:

FLEX 6000 Performance*				
BENCHMARK	LEs USED	-1 SPEED GRADE	-2 SPEED GRADE	-3 SPEED GRADE
16-bit loadable counter	16	140 MHz	131 MHz	109 MHz
16-bit accumulator	16	140 MHz	131 MHz	109 MHz
24-bit accumulator	24	108 MHz	103 MHz	86 MHz
16-to-1 multiplexer (pin-to-pin)	10	10.5 ns	11.7 ns	15.5 ns
16 x 16 multiplier, 4-stage pipeline	592	78 MHz	69 MHz	59 MHz
8-bit, 16-tap parallel finite impulse response (FIR) filter	599	94 MSPS	81 MSPS	67 MSPS
8-bit, 512-point fast Fourier transform (FFT)	1,182	75 μ S 62 MHz	87 μ S 54 MHz	109 μ S 43 MHz
a16450 universal asynchronous receiver/transmitter (UART)	468	36 MHz	30 MHz	25 MHz
PCI bus target with zero wait states	601	62 MHz	52 MHz	39 MHz

* Designs implemented in EPF6016A device and compiled using Altera MAX+PLUS® II version 9.0 software.

- In-circuit reconfigurability (ICR) is available via an external Configuration EPROM or intelligent controller
- Devices are fully compliant with the peripheral component interconnect (PCI) standard
- Built-in JTAG boundary-scan testing (BST) circuitry simplifies device- and system-level testing
- MultiVolt™ I/O interface makes FLEX 6000 devices ideal for 2.5-, 3.3-, and 5.0-V mixed-voltage systems
- One output enable per I/O pin supports flexible interrupt structures



Placement & Routing Efficiency with Fast Compilation Times

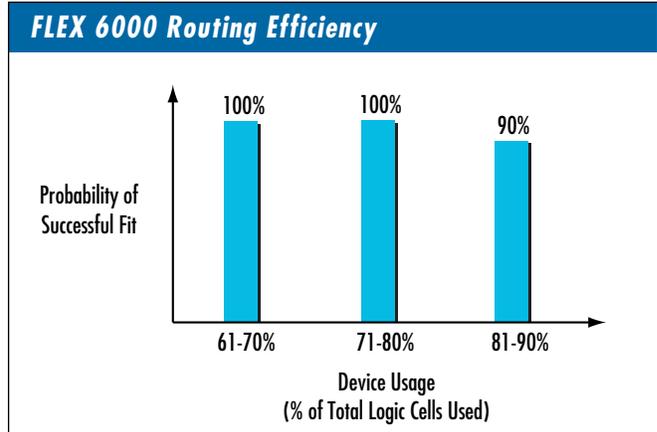
To help you quickly design with FLEX 6000 devices, Altera offers the most powerful, flexible, and easy-to-use development tools in the industry. The MAX+PLUS® II development software leverages the efficiency of the OptiFLEX architecture by offering the most automatic and sophisticated placement and routing algorithms. This combination of efficient device architecture and intelligent software algorithms allows the system designer to achieve desired place and route results within a matter of minutes while using a high percentage of the device's resources.

Design Flow Integration

MAX+PLUS II can exchange netlists in EDIF, VHDL, or Verilog HDL formats, providing a convenient interface to industry-standard EDA tools. Through the Altera Commitment to Cooperative Engineering Solutions (ACCESSSM) program, Altera supports design entry, synthesis, and simulation tools from all major EDA vendors, allowing FLEX 6000 devices to be integrated seamlessly into a designer's existing design environment.

Megafunction and Intellectual Property Support

To maximize design productivity, Altera provides complex system-level functions that are optimized for the FLEX 6000 architecture. Altera's MegaCore™ functions are developed, pre-tested, and licensed by Altera, providing customers with functions for PCI, UARTs, FFTs and more. Megafunctions are also offered through the Altera Megafunction Partners Program (AMPPSM), an



alliance between Altera and developers of synthesizable megafunctions. The AMPP alliance provides a broad portfolio of Altera-optimized megafunctions that facilitate high-density design.

FLEX 6000: Low Cost. Flexible. Fast Time-to-Market.

The FLEX 6000 family of programmable logic devices provides designers with a programmable alternative to gate arrays for high-volume production. With the industry's most efficient architecture—the OptiFLEX architecture—the Altera FLEX 6000 family delivers the flexibility and time-to-market of programmable logic at prices that are competitive with gate arrays.

Call Altera today or visit the web site at <http://www.altera.com> to learn more about how the FLEX 6000 family can provide low-cost flexibility for your volume production needs.

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