

Introduction

A critical element of system reliability is the capacity of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

You should complete a power evaluation early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature. This application note discusses how to evaluate and manage power, and provides sample worksheets for performing a power evaluation.

Power Evaluation

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, perform the following steps:

1. Estimate the power consumption of the application.
2. Calculate the maximum power for the device and package.
3. Compare the estimated and maximum power values.

Estimating Power Consumption

Use the following formula to compute the estimated power consumption (P_{EST}) of the application:

$$P_{EST} = P_{INT} + P_{IO}$$

$$\begin{aligned}\text{Where: } P_{INT} &= I_{CCINT} \times V_{CCINT} \\ P_{IO} &= P_{ACOUT} + P_{DCOUT}\end{aligned}$$

Therefore:

$$P_{EST} = (I_{CCINT} \times V_{CCINT}) + (P_{ACOUT} + P_{DCOUT})$$

The no-load power (P_{INT}) value can be obtained from the “Power Consumption” section in each device family data sheet. Because this value is “unloaded,” it is necessary to add the power dissipated by the I/O buffers— P_{DCOUT} from steady-state outputs and the P_{ACOUT} current from frequently switching outputs. P_{DCOUT} depends on the number of steady-state outputs, the logic levels they drive, and the resistive load on each output, as shown in the following formula:

$$P_{DCOUT} = \sum_{n=1}^d P_{DCn}$$

Where: d = Number of DC outputs
 P_{DCn} = DC output power of output n
 V_n = Voltage swing of output n
 f_n = Switching frequency of output n

Table 1 shows the DC power dissipated by the output drivers of a device with V_{CCIO} set at 5 V under typical types of loads. The DC power dissipated by the output driver does not equal the $V_{CC} \times I_{CCIO}$ value because most of the DC power is consumed by the load. If you are using a 3.3-V device or a non-5.0-V V_{CCIO} , you can compute the power based on the device’s I_{OH} and I_{OL} figures shown in the device family data sheet.

Table 1. DC Power Dissipated	
Load Driven	P_{DCn} (mW)
1-K pull-up resistor for low outputs	0.49
1-K pull-down resistor for high outputs	5.04
Bipolar for low outputs	0.16
Bipolar for high outputs	0.0576
CMOS inputs	Negligible

P_{ACOUT} depends on the capacitive load on each output and the frequency at which each output switches, as shown in the following formula:

$$P_{ACOUT} = \sum_{n=1}^a C_n V_n f_n \times V_{CCIO}$$

Where: a = Number of AC outputs
 C_n = Capacitive load on output n
 V_n = Voltage swing of output n
 f_n = Switching frequency of output n

The following equation shows the frequency of each output (f_n), in terms of the maximum clock frequency (f_{MAX}) of the design and the average ratio of I/O pins (tog_{IO}) toggling at each clock:

$$f_n = (0.5) \times f_{\text{MAX}} \times \text{tog}_{\text{IO}}$$

Inserting the equation for f_n into the P_{ACOUT} equation and resolving the summation for an average capacitive load yields the following formula:

$$P_{\text{ACOUT}} = (0.5) \times \text{OUT} \times C_{\text{AVE}} \times V_{\text{O}} \times f_{\text{MAX}} \times \text{tog}_{\text{IO}} \times V_{\text{CCIO}}$$

Where: OUT = Total number of output and bidirectional pins

Table 2 shows the V_{CCIO} and V_{O} values for Altera devices.

Table 2. V_{CCIO} & V_{O} Values	
V_{CCIO} (V)	V_{O} (V)
5.0	3.8
3.3	3.3
2.5	2.5

For example, the following equation provides the capacitive load for applications with $V_{\text{CCIO}} = 5 \text{ V}$:

$$P_{\text{ACOUT}} = (0.5) \times \text{OUT} \times C_{\text{AVE}} \times 3.8 \text{ V} \times f_{\text{MAX}} \times \text{tog}_{\text{IO}} \times 5.0 \text{ V}$$

Calculating Maximum Power for the Device & Package

The following formulas are used to calculate the maximum allowed power (P_{MAX}) for a device:

$$P_{\text{MAX}} = \frac{T_{\text{J}} - T_{\text{A}}}{\theta_{\text{JA}}} \quad \text{or} \quad P_{\text{MAX}} = \frac{T_{\text{J}} - T_{\text{C}}}{\theta_{\text{JC}}}$$

The maximum allowed power is dependent on the maximum allowed junction temperature (T_J) of the silicon, the ambient temperature of operation (T_A), and the package's thermal resistance (θ_{JA}) when configured in the system. The maximum junction temperature is specified in the Altera® device family data sheets. The ambient temperature depends on the application. The worst-case P_{MAX} value is estimated using the formula with θ_{JA} , the junction-to-ambient thermal resistance. The θ_{JA} value for Altera devices is provided for still air (with convection cooling only), and for a forced-air flow of 100 feet/second, 200 feet/second, and 400 feet/second. If heat-sinking is used to dissipate heat and θ_{JA} for a heat sink is given, you should use the case temperature (T_C) and the junction-to-case thermal resistance (θ_{JC}) to calculate P_{MAX} for a device. θ_{JC} is a measure of the lowest possible thermal resistance.



For thermal resistance values (θ_{JC} and θ_{JA}) of Altera devices, refer to the *Altera Device Packaging Information Data Sheet* in this data book.

Comparing Maximum Allowed Power & Estimated Power

To avoid reliability problems, you should compare the values calculated for the maximum allowed power and estimated power. The estimated power should be the smaller of the two values. If the estimated power exceeds the maximum allowed power, refer to “[Thermal Management](#)” on page 509 for suggestions on how to reduce power requirements for a design. [Figure 1](#) shows a sample worksheet for evaluating power.

Figure 1. Power Evaluation Worksheet (Part 1 of 2)

Design _____ Device _____

Estimating the Power Consumption of the Application**Internal Power Calculation for All Altera Devices***FLEX 10K, FLEX 8000 & FLEX 6000 Devices*Standby current (I_{CC0}) _____ $I_{CC0} =$ _____ mACoefficient for I_{CC} calculation. See the appropriate device family data sheet for this value. $K =$ _____ $\mu A/(MHz \times LE)$ Maximum clock frequency (f_{MAX}) _____ $f_{MAX} =$ _____ MHz

Total number of logic elements (LEs) used in the device (N) _____

 $N =$ _____ LEAverage ratio of logic cells toggling (**tog_{LC}**) at each clock (typically 0.125) _____**tog_{LC}** = _____Total internal current (I_{CCINT}) _____ $I_{CCINT} =$ _____ mA

$$I_{CCINT} = I_{CC0} + K \times f_{MAX} \times N \times \text{tog}_{LC}$$

Total internal power (P_{INT}) _____ $P_{INT} =$ _____ mW

$$P_{INT} = V_{CC} \times I_{CCINT}$$

*MAX 9000 & MAX 7000 Devices*Coefficients for I_{CC} calculation. See the appropriate device family data sheet for these values. $A =$ _____ mA/LE $B =$ _____ mA/LE $C =$ _____ mA/(MHz $\times$ LE)Number of macrocells with the Turbo Bit on (MC_{TON}) _____ $MC_{TON} =$ _____ LENumber of macrocells in the device (MC_{DEV}) _____ $MC_{DEV} =$ _____ LENumber of macrocells in the design (MC_{USED}) _____ $MC_{USED} =$ _____ LEMaximum clock frequency (f_{MAX}) _____ $f_{MAX} =$ _____ MHzAverage ratio of logic cells toggling (**tog_{LC}**) at each clock (typically 0.125) _____**tog_{LC}** = _____Total internal current (I_{CCINT}) _____ $I_{CCINT} =$ _____ mA

$$I_{CCINT} =$$

$$(A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times f_{MAX} \times \text{tog}_{LC})$$

Total internal power (P_{INT}) _____ $P_{INT} =$ _____ mW

$$P_{INT} = V_{CC} \times I_{CCINT}$$

External Power Calculation for All Altera DevicesPower consumed by the DC output load (P_{DCOUT}) _____ $P_{DCOUT} =$ _____ mW

$$P_{DCOUT} = P_{DCn}$$

Average capacitive load (C_{AVE}) at output pins _____ $C_{AVE} =$ _____ pF

Number of output/bidirectional pins in the design (OUT) _____

OUT = _____

Average ratio of I/O pins toggling (**tog_{IO}**) at each clock (typically 0.125) _____**tog_{IO}** = _____Power consumed by AC output load (P_{ACOUT}) _____ $P_{ACOUT} =$ _____ mW

$$P_{ACOUT} = 1/2 \times OUT \times C_{AVE} \times V_O \times f_{MAX} \times \text{tog}_{IO} \times V_{CCIO} \times 0.001$$

Total external power (P_{IO}) _____ $P_{IO} =$ _____ mW

$$P_{IO} = P_{DCOUT} + P_{ACOUT}$$

Figure 1. Power Evaluation Worksheet (Part 2 of 2)

Total Power Calculation for All Altera Devices

Estimated total power (P_{EST}) $P_{EST} = \rule{1cm}{0.4pt} \text{ mW}$
 $P_{EST} = P_{INT} + P_{IO}$

Calculating Maximum Allowed Power for the Device & Package

Thermal resistance of the device $\theta_{JA} = \rule{1cm}{0.4pt} \text{ }^{\circ}\text{C/W}$
Maximum junction temperature (T_J) as specified in the appropriate device $T_J = \rule{1cm}{0.4pt} \text{ }^{\circ}\text{C}$
family data sheet.

Ambient temperature (T_A) of the design $T_A = \rule{1cm}{0.4pt} \text{ }^{\circ}\text{C}$
Maximum power (P_{MAX}) allowed for the device $P_{MAX} = \rule{1cm}{0.4pt} \text{ W}$
 $P_{MAX} = (T_J - T_A)/\theta_{JA}$

Comparing Maximum Power Allowed & Estimated Power

Is $P_{EST} < P_{MAX}$? Yes or No

Tables 3 and 4 show design parameters for the sample power evaluations shown in Figures 2 and 3. The design parameters are unique to the sample designs and are not found in device family data sheets.

Table 3. Parameters for the Sample FLEX 10K Design		
Parameter	Description	Value
OUT	Number of outputs	150
Number of 1-KΩ pull-up resistors	Type of load	50
CMOS inputs	Type of load	100
C _{AVE}	Average capacitance	35 pF
N	Number of logic elements used	2,747 LE
f _{MAX}	Maximum operating frequency	20 MHz
P _{DCOUT}	Static power consumed by outputs	(0.49 mW × 50) + (0 mW × 231) = 24.5 mW

Table 4. Parameters for the Sample MAX 9000 Design

Parameter	Value
MC _{TON}	139
MC _{DEV}	560
MC _{USED}	500
MC _{TOFF}	421
f _{MAX}	40 MHz
OUT	211
Number of 1-K Ω pull-down resistors	10
CMOS inputs	201
C _{AVE}	35 pF
P _{DCOUT}	$(5.04 \text{ mW} \times 10) + (0 \text{ mW} \times 201) = 50 \text{ mW}$

Figures 2 and 3 provide power evaluations for sample designs implemented in FLEX[®] 10K and MAX[®] 9000 devices, respectively.

Figure 2. Sample Power Evaluation for a FLEX 10K Device (Part 1 of 2)

Design dsp_fir.tdf Device EPF10K50VBC356-2

Estimating the Power Consumption of the Application

Internal Power Calculation

FLEX 10K, FLEX 8000 & FLEX 6000 Devices

Standby current ($I_{CCSTANDBY}$)	$I_{CCSTANDBY} =$	<u>0.500</u>	mA
Coefficient for I_{CC} calculation. See the appropriate device family data sheet for this value.	$K =$	<u>45</u>	$\mu A/(MHz \times LE)$
Maximum clock frequency (f_{MAX})	$f_{MAX} =$	<u>50</u>	MHz
Total number of logic elements used in the device (N)	$N =$	<u>2,747</u>	LE
Average ratio of logic cells toggling (tog_{LC}) at each clock (typically 0.125)	$tog_{LC} =$	<u>0.125</u>	
Total internal current (I_{CCINT})	$I_{CCINT} =$	<u>773.09</u>	mA
$I_{CCINT} = I_{CCSTANDBY} + K \times f_{MAX} \times N \times tog_{LC}$			
Total internal power (P_{INT})	$P_{INT} =$	<u>2,551.2</u>	mW
$P_{INT} = V_{CC} \times I_{CCINT}$			

External Power Calculation for All Altera Devices

Power consumed by the DC output load (P_{DCOUT})	$P_{DCOUT} =$	<u>35</u>	mW
$P_{DCOUT} = P_{DCn}$			
Average capacitive load (C_{AVE}) at output pins	$C_{AVE} =$	<u>35</u>	pF
Number of output/bidirectional pins in the design (OUT)	$OUT =$	<u>150</u>	
Average ratio of I/O pins toggling (tog_{IO}) at each clock (typically 0.125)	$tog_{IO} =$	<u>0.125</u>	
Power consumed by AC output load (P_{ACOUT})	$P_{ACOUT} =$	<u>178.66</u>	mW
$P_{ACOUT} = 1/2 \times OUT \times C_{AVE} \times 3.3 V \times f_{MAX} \times tog_{IO} \times 3.3 V \times 0.001$			
Total external power (P_{IO})	$P_{IO} =$	<u>213.66</u>	mW
$P_{IO} = P_{DCOUT} + P_{ACOUT}$			

Total Power Calculation for All Altera Devices

Estimated total power (P_{EST})	$P_{EST} =$	<u>2,764.9</u>	mW
$P_{EST} = P_{INT} + P_{IO}$			

Figure 2. Sample Power Evaluation for a FLEX 10K Device (Part 2 of 2)**Calculating Maximum Allowed Power for the Device & Package**

Thermal resistance of the device

$$\theta_{JA} = \frac{8}{}^{\circ}\text{C/W}$$

Maximum junction temperature (T_J) as specified in the appropriate device family data sheet.

$$T_J = \frac{85}{}^{\circ}\text{C}$$

Ambient temperature (T_A) of the design

$$T_A = \frac{40}{}^{\circ}\text{C}$$

Maximum power (P_{MAX}) allowed for the device

$$P_{MAX} = \frac{5.625}{}\text{W}$$

$$P_{MAX} = (T_J - T_A)/\theta_{JA}$$

Comparing Maximum Power Allowed & Estimated PowerIs $P_{EST} < P_{MAX}$?☒ Yes or No

Figure 3. Sample Power Evaluation for a MAX 9000 Device (Part 1 of 2)

Design atm_pkt.tdf Device EPM9560ARC304-15

Estimating the Power Consumption of the Application

Internal Power Calculation

MAX 9000 & MAX 7000 Devices

Coefficients for I_{CC} calculation. See the appropriate device family data sheet for these values.

Number of macrocells with the Turbo Bit on (MC_{TON})

Number of macrocells in the device (MC_{DEV})

Number of macrocells in the design (MC_{USED})

Maximum clock frequency (f_{MAX})

Average ratio of logic cells toggling (tog_{LC}) at each clock (typically 0.125)

Total internal current (I_{CCINT})

$$I_{CCINT} = (A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times f_{MAX} \times tog_{LC})$$

Total internal power (P_{INT})

$$P_{INT} = V_{CC} \times I_{CCINT}$$

A = 0.68 mA/LE
B = 0.26 mA/LE
C = 0.052 mA/(MHz × LE)

MC_{TON} = 139 LE
MC_{DEV} = 560 LE
MC_{USED} = 500 LE
f_{MAX} = 40 MHz
tog_{LC} = 0.125
I_{CCINT} = 333.98 mA

P_{INT} = 1,669.9 mW

External Power Calculation for All Altera Devices

Power consumed by the DC output load (P_{DCOUT})

$$P_{DCOUT} = P_{DCn}$$

Average capacitive load (C_{AVE}) at output pins

Number of output/bidirectional pins in the design (OUT)

Average ratio of I/O pins toggling (tog_{IO}) at each clock (typically 0.125)

Power consumed by AC output load (P_{ACOUT})

$$P_{ACOUT} = 1/2 \times OUT \times C_{AVE} \times 3.8 \text{ V} \times f_{MAX} \times tog_{IO} \times 5 \text{ V} \times 0.001$$

Total external power (P_{IO})

$$P_{IO} = P_{DCOUT} + P_{ACOUT}$$

P_{DCOUT} = 50 mW

C_{AVE} = 35 pF
OUT = 211
tog_{IO} = 0.125
P_{ACOUT} = 350.79 mW

P_{IO} = 400.79 mW

Total Power Calculation for All Altera Devices

Estimated total power (P_{EST})

$$P_{EST} = P_{INT} + P_{IO}$$

P_{EST} = 2,070.69 mW

Calculating Maximum Allowed Power for the Device & Package

Thermal resistance of the device

Maximum junction temperature (T_J) as specified in the appropriate device family data sheet.

Ambient temperature (T_A) of the design

Maximum power (P_{MAX}) allowed for the device

$$P_{MAX} = (T_J - T_A) / \theta_{JA}$$

θ_{JA} = 8 °C/W
T_J = 90 °C

T_A = 70 °C
P_{MAX} = 2.5 W

Figure 3. Sample Power Evaluation for a MAX 9000 Device (Part 2 of 2)**Comparing Maximum Power Allowed & Estimated Power**Is $P_{EST} < P_{MAX}$?☒ Yes or No

Thermal Management

The following guidelines reduce power dissipation and heat build-up for an application:

- *Use available low-power features of the device.* By turning the Turbo Bit off, Classic devices and individual macrocells in MAX 9000, and MAX 7000 devices can be configured for low-power operation, with only a nominal increase in propagation delays. All macrocells in MAX 9000 or MAX 7000 devices that do not need to run in high-performance mode should be set to low-power mode.
- *Choose a different device package.* A ceramic or higher-pin-count package can be used. Ceramic packages dissipate more heat than plastic packages. Also, packages with higher pin counts can dissipate more heat through the connections to the printed circuit board (PCB). Finally, SuperBGA and power quad flat pack (RQFP) packages also dissipate heat.
- *Use forced-air cooling and/or heat-sinking.* Forced-air cooling improves the efficiency of convection cooling, which reduces the surface temperature of the device. A heat sink connected to a device significantly increases heat dissipation by radiating heat via the metal mass.
- *Slow the operation in portions of the circuit.* I_{CC} is proportional to the frequency of operation. Slowing parts of a circuit lowers the I_{CC} and hence reduces the power. Altera devices provide global or array clock sources for all registers. Signals that do not require high-speed operation can use a slower array clock that significantly reduces the system power consumption.
- *Reduce the number of outputs.* DC and AC current is required to support all I/O pins on the device. Reducing the number of I/O pins may reduce the current necessary for the device, and thereby reduce the power.

- *Reduce the amount of circuitry in the device.* Power depends on the amount of internal logic that switches at any given time. Reducing the amount of logic in a device reduces the current in the device. The same effect may be achieved by using a larger device, which also provides increased heat dissipation and maintains a single-device solution.
- *Choose a different device family.* Some device families consume less power than others. For example, the MAX 7000 family provides more power-saving features than the MAX 5000 family. The Classic family provides power-saving features for low-density designs, and low-speed designs consume less power when implemented in FLEX devices.
- *Modify the design to reduce power.* Identify areas in the design that can be revised to reduce the power requirements. Common solutions include reducing the number of switching nodes and /or required logic, and removing redundant or unnecessary signals. For assistance in locating less obvious changes, contact Altera Applications at (800) 800-EPLD.

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