APEX 20K

Programmable Logic Device Family

October 1998, ver. 1 | Advance Information Brief

Features...

- High-density, embedded programmable logic device (PLD) family designed for system-level integration
  - 100,000 to 1 million typical gates (see Table 1)
  - Up to 42,240 logic elements (LEs)
  - Up to 4,224 macrocells
  - Up to 540,672 memory bits
- MultiCore™ embedded architecture
  - Combines and enhances the strengths of the FLEX® 10K, FLEX 6000, and MAX® 7000 architectures
  - Integrates look-up table (LUT) logic, product-term logic, and memory into a single architecture
  - Facilitates efficient intellectual property (IP) integration
  - Four-level FastTrack Interconnect™ continuous routing structure for fast, predictable timing
- Advanced embedded system block (ESB)
  - 2,048 programmable bits per ESB
  - Configurable as product-term logic, LUT logic, RAM, ROM, or content addressable memory (CAM)
  - Cascadable to support larger functions

Preliminary Information

Table 1. APEX 20K Device Features *Note (1)*

Feature	EP20K100	EP20K160	EP20K200	EP20K300	EP20K400	EP20K600	EP20K1000
Maximum gates	263,000	404,000	526,000	728,000	1,052,000	1,537,000	2,670,000
Typical gates	53,000 to 106,000	82,000 to 163,000	106,000 to 211,000	147,000 to 293,000	213,000 to 423,000	311,000 to 618,000	541,000 to 1,073,000
LEs	4,160	6,400	8,320	11,520	16,640	24,320	42,240
Maximum macrocells	416	640	832	1,152	1,664	2,432	4,224
ESBs	26	40	52	72	104	152	264
Maximum RAM bits	53,248	81,920	106,496	147,456	212,992	311,296	540,672
Maximum user I/O pins	250	320	320	420	500	620	780

Note:
(1) The first APEX™ 20K devices are planned to be available in the first quarter of 1999.

…and More Features

- Embedded product-term logic
  - Ideal for wide fan-in control logic applications, such as address decoding and state machines
  - High-performance product-term delay
- High-performance dual-port RAM
  - Independent read/write ports
  - Synchronous or asynchronous access
  - 150-MHz first-in first-out (FIFO) performance
- Compliant with 3.3-V peripheral component interconnect (PCI) bus
  - APEX 20K devices support the PCI Special Interest Group's (PCI SIG) ***PCI Local Bus Specification, Revision 2.1***
  - 64-bit, 66-MHz performance
- Low-voltage I/O standard support
  - User-selectable support for low-voltage transistor-to-transistor logic (LVTTL), low-voltage CMOS (LVCMOS), Gunning transceiver logic (GTL/GTL+), stub-series terminated logic (SSTL-3), and low-voltage differential signaling (LVDS) interface standards
- Enhanced phase-locked loop (PLL)
  - ClockBoost™ circuitry for 1×, 2×, and 4× clock multiplication
  - ClockLock™ synchronization circuitry: 1 MHz to 200 MHz output frequency range
- Advanced process technology
  - Fabricated on a 0.25-µm, six-layer-metal CMOS SRAM process with planned migration to a 0.18-µm process
  - MultiVolt™ I/O interface supports 1.8-V, 2.5-V, and 3.3-V mixed-voltage systems
- 1.0-mm and 0.8-mm FineLine BGA™ packaging requiring half the board area of traditional ball-grid array (BGA) packages
- Software design support and automatic place-and-route provided by Altera's fourth-generation development system—the Quartus™ software—on Pentium-based PCs and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations

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